

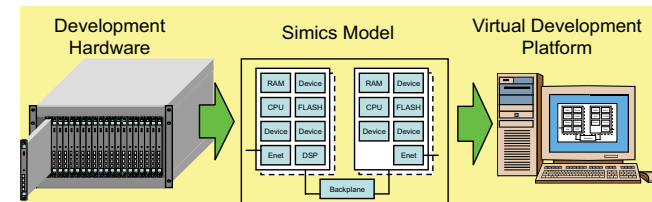
What is Virtualized System Development?

Dan Ekblom, PhD
Senior Application Engineer



Virtutech Simics

- **Full system simulation**
 - Complete machines, networks, backplanes
 - System-level from the beginning
- **Runs complete software stack**
 - Firmware, device drivers, OS, hypervisor, etc...
- **Very high performance**
 - Typically 100s of MIPS
 - Multiple GIPS top benchmark



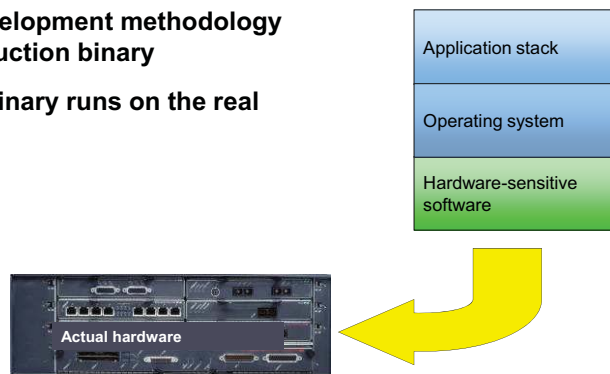
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Traditional System Development

- **Software development methodology creates production binary**
- **Production binary runs on the real hardware**



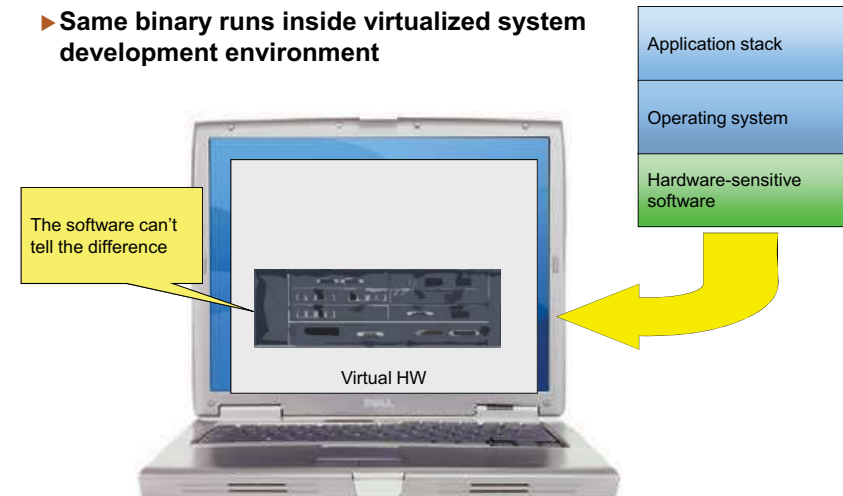
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Virtualized System Development

- **Same binary runs inside virtualized system development environment**

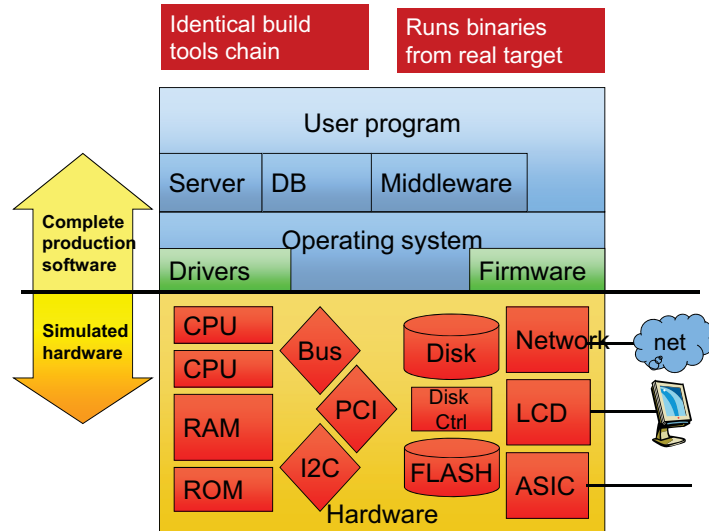


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What is modeled in VSD?

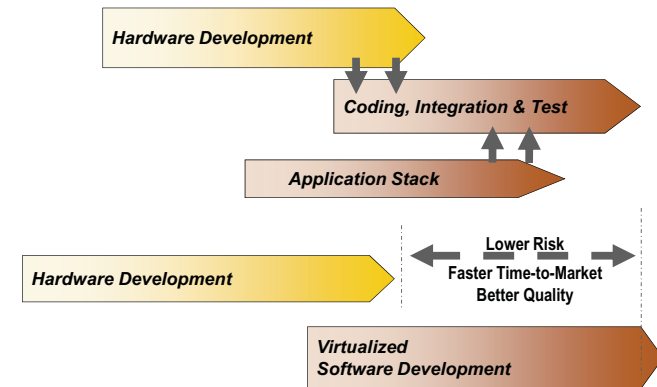


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Virtualized System Development: Enables Changes!



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Customer Experience

"Simulation is the key to advanced microprocessor development, and Simics is by far the most advanced realization of this technology available. Our vision is to eventually simulate the entire code stack from firmware up, and Virtutech's Simics will be the cornerstone of this development."

Kevin Collins, Director, Global Firmware Development, IBM



"Debug with Simics is 4-8 times faster than with hardware"

Tracy Bashore, Manager SLIC storage management development, IBM

"Simics is really the only way to develop multi-core software"

Tomas Evensen, CTO, WindRiver



"The processing potential of multi-core devices remains untapped because multicore systems are only as effective as software's ability to handle parallelism"

Chekib Akrou, VP & GM Networking System Division, Freescale



"Simics allows us to test our software and validate it while the underlying hardware design is being"

Gerry Vossler, VP, Advanced Marketing & Technology



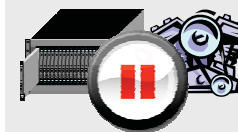
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In the virtual world, anything is possible

Synchronous stop for entire system



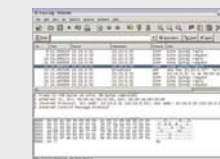
Unlimited and powerful breakpoints

```
break -x 0x0000->0x1F00
break-io uart0
break-exception int13
```

Determinism and repeatability



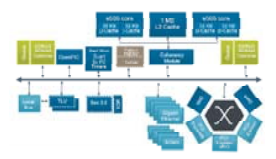
Trace anything



Reverse execution



Insight into all devices



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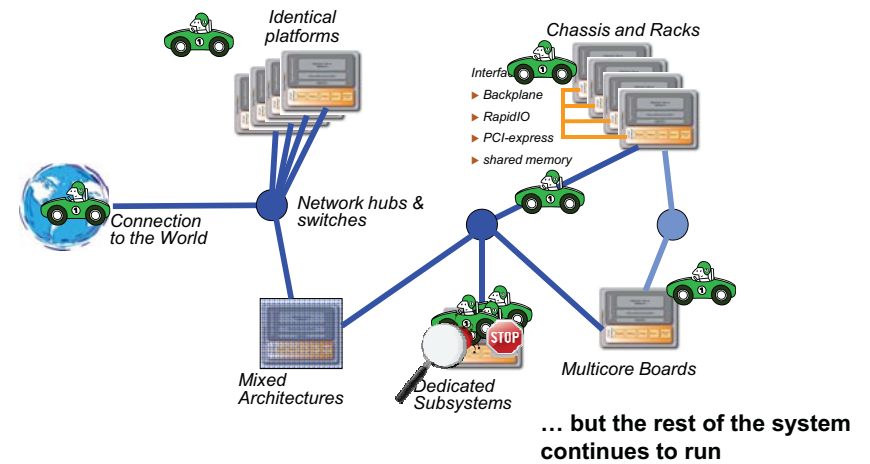
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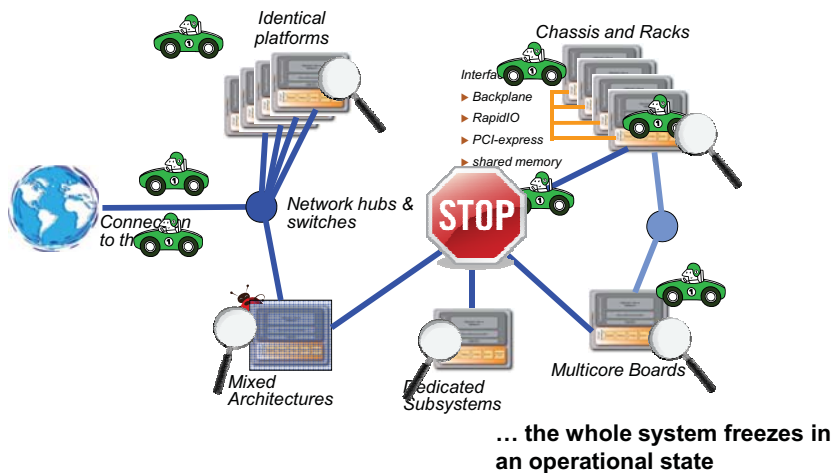
SYSTEM STOP

The entire system can be stopped, inspected and debugged at any time

Traditional debug: A Single Component may stop ...



VSD debugging: Synchronized System Stop

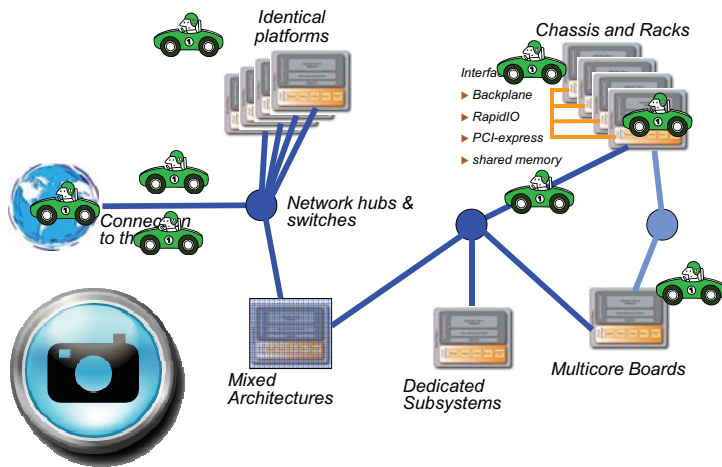


SYSTEM CHECKPOINTS

A virtual system can be frozen, captured, and restored at any time, location or computer

... without replication errors

Taking a Check Point



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Sending the Check Point



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Restore and Run



Restore the checkpoint and resume

- At any time
- In any location
- On any computer

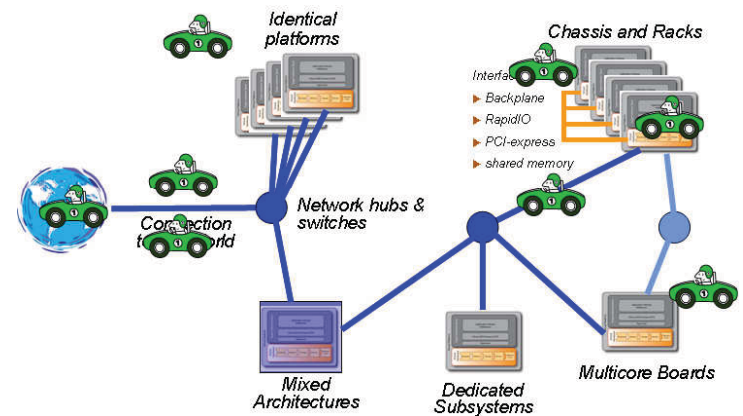


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Restore and Run

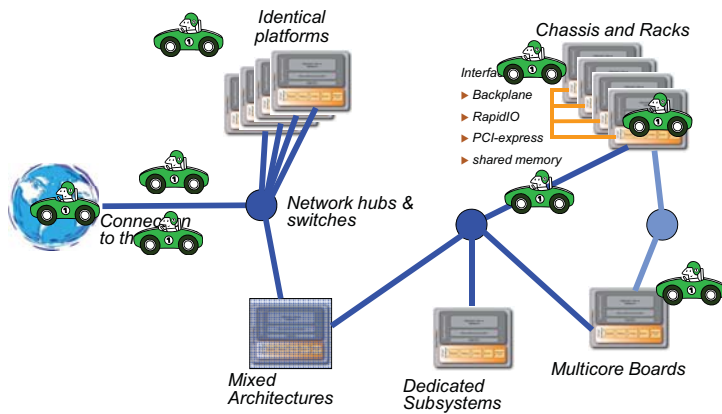


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Restore and Run



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RUN TO RUN REPEATABILITY

The “path” taken through code execution is repeated on every run (determinism)

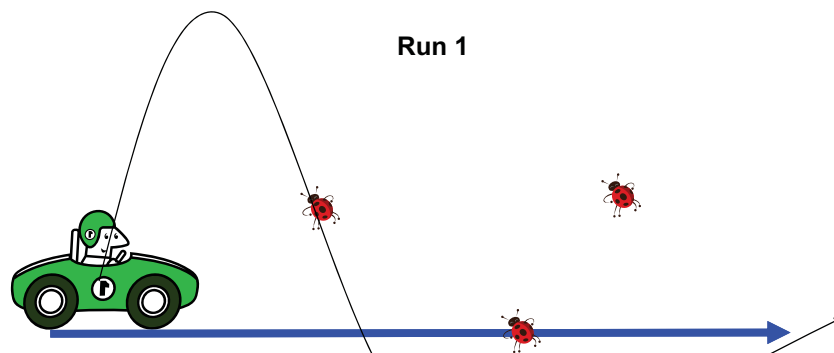
... until stimuli are specifically modified

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Repeatability - Traditional Hardware



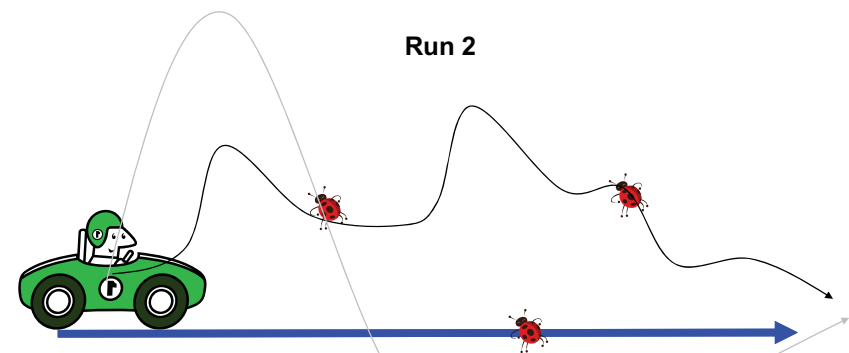
- Physical systems are not wholly predictable or controllable
- The system will usually follow a slightly different path from start to finish
- Some runs will hit bugs, others will not.

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Repeatability - Traditional Hardware



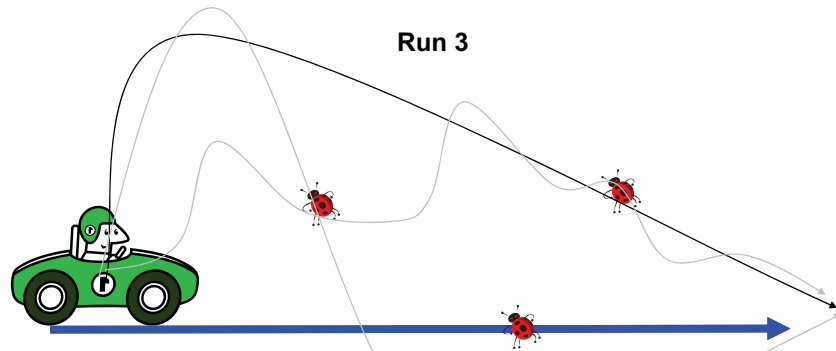
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Repeatability - Traditional Hardware



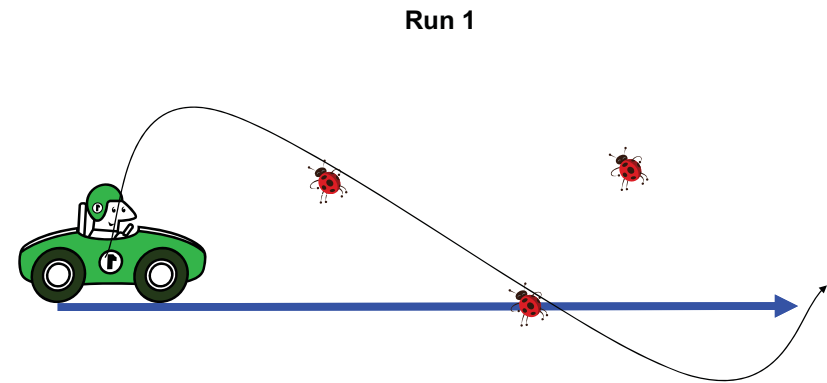
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Repeatability – Virtual Hardware



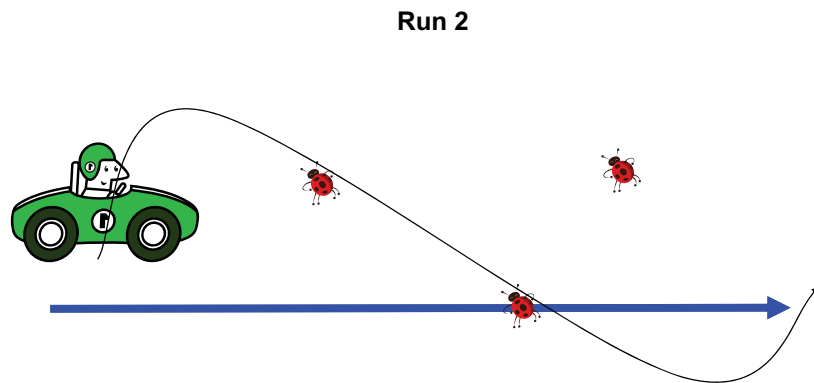
- Simics virtual platforms are predictable and controllable
- The system will follow exactly the same path from start to finish
 - Every developer will precisely duplicate every execution step

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Repeatability – Virtual Hardware



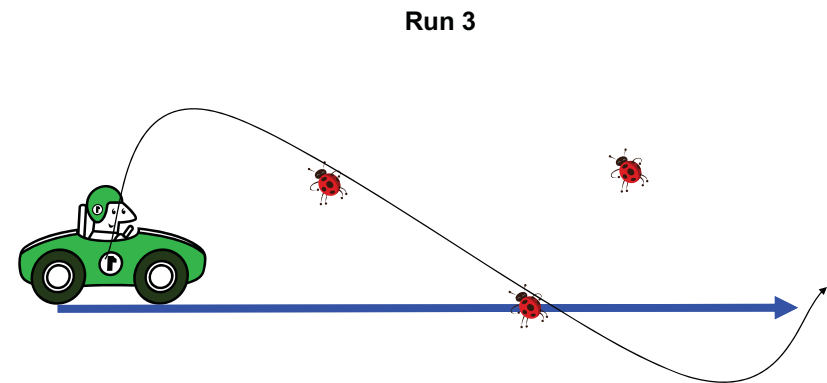
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Repeatability – Virtual Hardware



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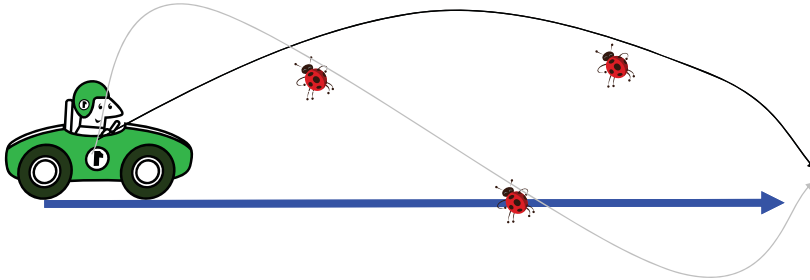
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Repeatability – Virtual Hardware

Run 4 (new stimuli)



- New stimuli can be injected to ensure different paths
- Random paths can be generated

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DEBUGGING THE SYSTEM

Physical systems can only run forward

... requires traditional iterative debug approaches

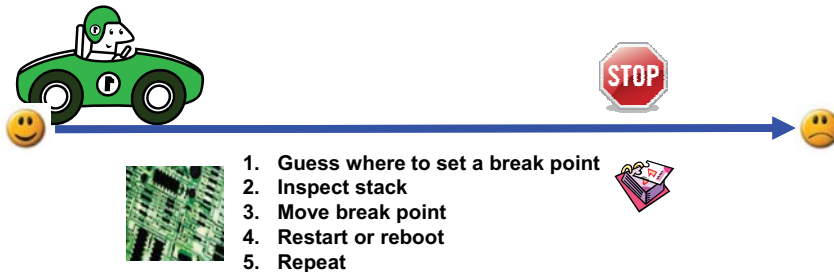
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Iteratively Converging on the Problem

Traditional Hardware Debug



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Iteratively Converging on the Problem

Traditional Hardware Debug



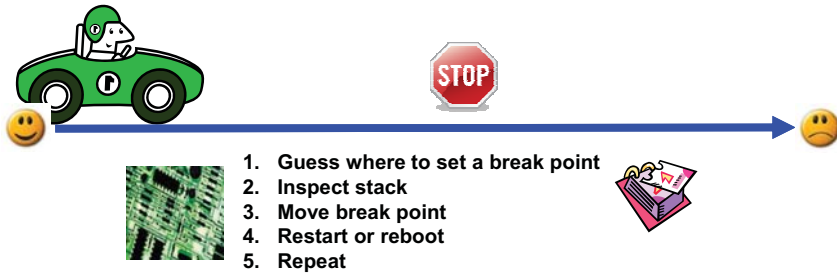
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Iteratively Converging on the Problem

Traditional Hardware Debug



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Iteratively Converging on the Problem

Traditional Hardware Debug



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Iteratively Converging on the Problem

Traditional Hardware Debug



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Iteratively Converging on the Problem

Traditional Hardware Debug



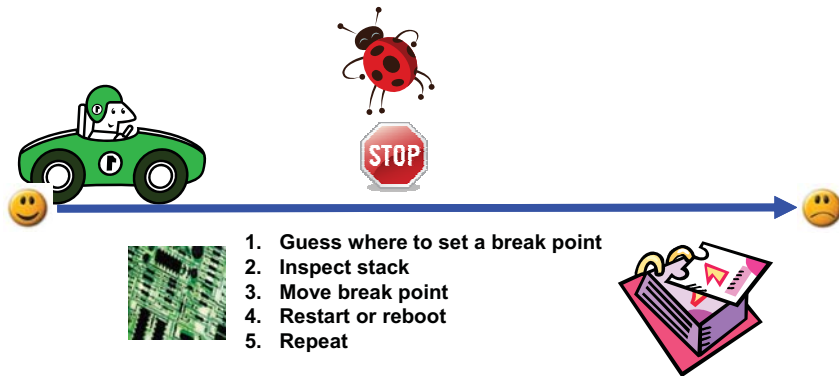
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Iteratively Converging on the Problem

Traditional Hardware Debug



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REVERSE EXECUTION

A system runs backwards, through every operation and breakpoint along the way

A new paradigm to debug and investigate problems

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Linearly Converging on the Problem

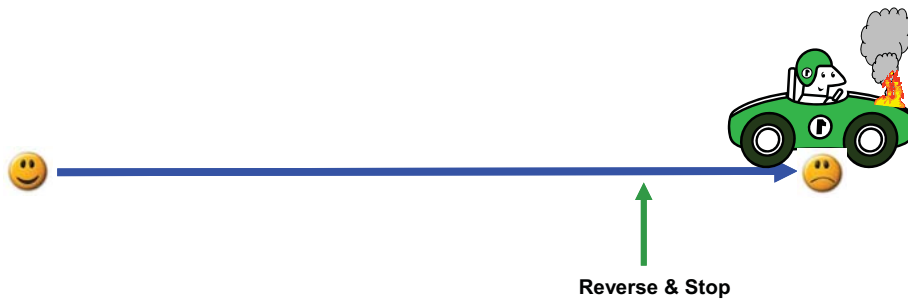
VSD Debug

Stack

GGGGGGBBBBB

Stack is now at the last known bad point

- Begin after the problem occurs
- Set breakpoint on OS kill signal
- Run in reverse up to breakpoint



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Linearly Converging on the Problem

VSD Debug

Stack

GGGGGGGGBBBB

Stack is known bad at this point

While observing the stack, run in reverse, stopping at breakpoints along the way



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Linearly Converging on the Problem

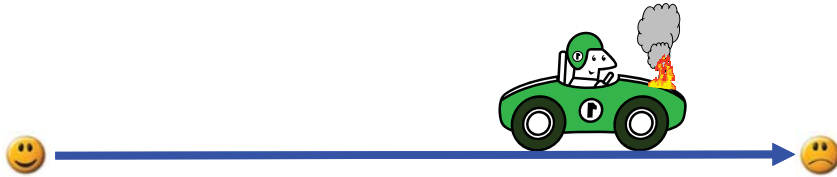
VSD Debug

Stack

GGGGGGGG BB

Stack is known bad at this point

While observing the stack, run in reverse, stopping at breakpoints along the way



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Linearly Converging on the Problem

VSD Debug

Stack

GGGGGGGG BB

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While observing the stack, run in reverse, stopping at breakpoints along the way



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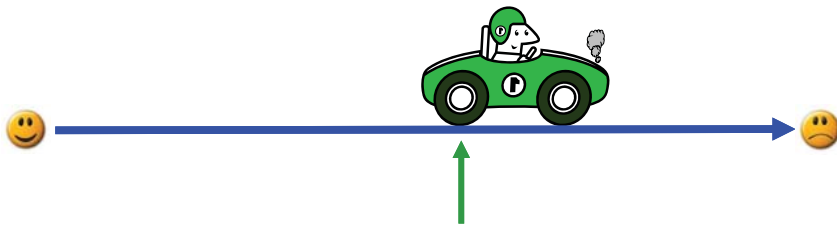
Linearly Converging on the Problem

VSD Debug

Stack

GGGGGGGGGG B

Now, set a watchpoint on the corrupt variable and resume reverse execution.



This is where the first bad stack frame appears

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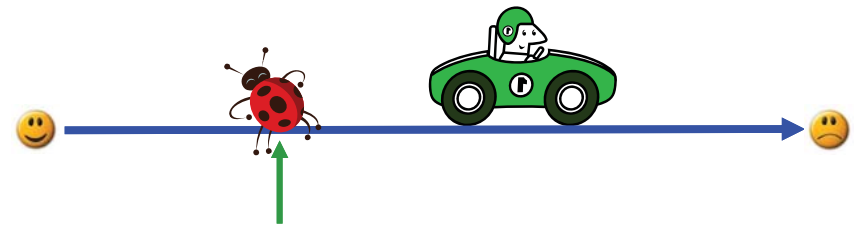


Linearly Converging on the Problem

VSD Debug

Stack

GGGGGGGGGG



- Watchpoint triggers & execution stops
- Debugger points to offending line of source code.

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Virtual Systems Development - Summary

- ▶ Reduces the risk in software projects, decouples hardware and software development
- ▶ Very efficient platform for full system multisystem/multicore debug

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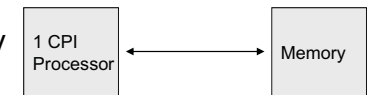
Virtual Systems Development - Summary

- ▶ Reduces the risk in software projects, decouples hardware and software development
- ▶ Very efficient platform for full system multisystem/multicore debug
- ▶ Also possible to use Simics for architectural exploration:
 - Adding more cores
 - Comparing different architectures
 - Adding cache models
 - The limit is the sky...

Cache Modeling in Simics

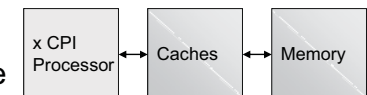
Basic model

1 instr = 1 cycle
No cache, perfect memory
100+ MIPS speed



Cache model

Compute instr = 1 cycle
Memory instr = cache time
Cache statistics & traces
1+ MIPS speed





What is Virtualized System Development?

Dan Ekblom, PhD
Senior Application Engineer

