# Hardware transactional memory in HPC applications


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**Handle concurrency in a new way**
Hardware transactional memory (HTM) provide a convenient solution of protecting your critical code sections from concurrency issues.

CHKPT

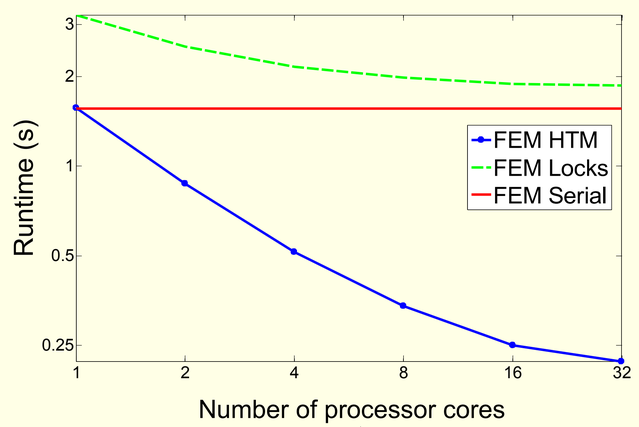
**Investigation of suitable HPC applications**
We have investigated the suitability of various applications. Assembly of a stiffness matrix and molecular dynamics simulation was then tested on prototype hardware with HTM support and an accompanying experimental compiler.

CONFLICT

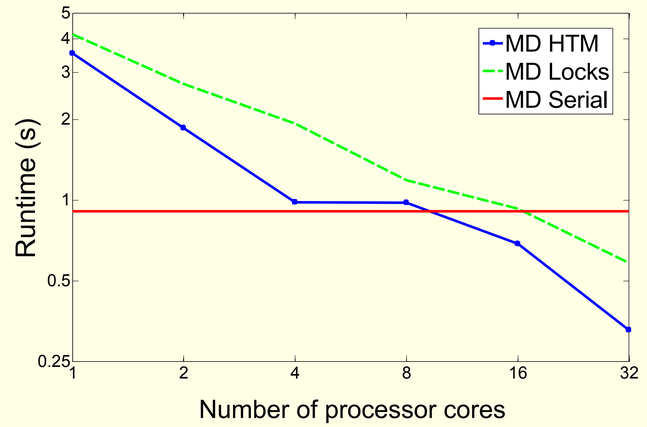
**Can simplify coding**
HTM reduces the need for using locks, making - in theory - the code easier to construct and read. At present day however, the lack of HTM support among compilers is a limitation.

GO TO FAILPC

**Scaling of FEM matrix assembly**




**Scaling of molecular dynamic simulation**




**Can increase performance**
The performance of HTM is very application dependent. Assembling of some FEM matrices are tasks that suit HTM very well, and it outperforms the corresponding lock implementation.

A simple MD simulation also shows that HTM has potential to scale well. However, the execution time of the MD implementation varies widely. We have not yet determined if this is due to the HTM implementation or software shortcomings.

COMMIT

**Future work**
The results attained show that there is potential in HTM for certain HPC applications. More thorough tests and a larger application set is required to make a final verdict in the future use of HTM in HPC programs.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