

## **Master Thesis: High level synthesis tool for high speed packet processing**

*Suitable for two master thesis students*

### **Background**

Ethernet is already the preeminent network technology used anywhere from home networks to the Internet. The next logical step is to replace the specialized networks previously seen in niches such as cars, super computers and data-centers with Ethernet. However, this development requires that the next generation of Ethernet equipment can handle the vast span of features and performance requirements seen in these niches.

The aim of this Masters Thesis is to find a way of delivering the needed performance and features for packet processing without resorting to a custom RTL design for each network niche.

The art of packet processing is comprised of two parts: Finding out the local destination for a network packet, and performing alterations to the packet. It is usually done in four steps:

- First the packet is inspected, the packet type is determined and the relevant data for the packet type is extracted.
- Second, the local destination is determined by looking up the extracted data in a number of tables. There may also be packet alterations decided in this step.
- Third, egress specific table lookups are made when the packet has reached the local destination output port.
- The fourth and final packet processing step is to modify the packet according to the instructions assembled in the previous steps.

The industry norm is to implement the packet processing as hard-coded RTL using a hardware description language such as Verilog or VHDL. However the problem seems to possess sufficient regularity to be a candidate for high level synthesis.

### **Work to be carried out**

1. Device a customized high level Packet Processing Language (PPL) where the packet processing can be described in a simple yet powerful way.
2. Build a compiler for the PPL, capable of generating a timeless executable model and a synthesizable RTL model.

### **Suggested work order**

- Study existing research in the field
- Study the packet processing in a few typical network devices
- Design the PPL language primitives
- Implement and verify the PPL compiler

### **Useful skills**

- Network protocols such as Ethernet, IPv4/IPv6 and TCP/UDP
- Hardware design in Verilog or VHDL
- Programming (C++ or Python for instance)
- Linux know-how

### **Packet Architects AB**

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