Master Thesis: ASIC Generator for network cards & switches

Suitable for two master thesis students

Background
Ethernet is already the preeminent network technology used anywhere from home networks to the Internet. The next logical step is to replace the specialized networks previously seen in niches such as cars, super computers and data-centers with Ethernet. However, this development requires that the next generation of Ethernet equipment can handle the vast span of features and performance requirements seen in these niches.

Todays home, office, data-center, corporate networks and carrier (telco) networks all use the same types of chip-designs but with slightly different number of ports and total bandwidth. Another trend is that a server today runs a number of virtual machines (number of OS's in parallel) and network cards therefore located inside the servers of todays data-centers are getting more and more complex and act like a small switch thereby a network card of today has a similar functionality as a switch would have.

Work to be carried out
A generic switching architecture should be able to handle a set of different options which would allow a single design with the help of steering files to be configured either as a switch with a set of ports or a network card with a different set of requirements. The work is to define the high level steering files, and the build a generator to turn those steering files into a design in a HDL language (Verilog).

There exists many ways to build a generic design today, either use the a pre-processor, use a higher level language, use primates in existing HDL languages or use a script-based language.

Suggested work order
- Study existing research in this field of generating designs (CPU's are mostly common)
- Try out different ways to generate a design to determine to determine best way forward
- Study the architecture of the Ethernet switching chips
- Implement and verify the design generator
- Write report

Good to have knowledge
- Understanding of network protocols such as Ethernet, IPv4/IPv6 and TCP/UDP
- Understanding of hardware design in Verilog/VHDL
- Programming in C / C++ / Python etc.
- Linux know-how

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