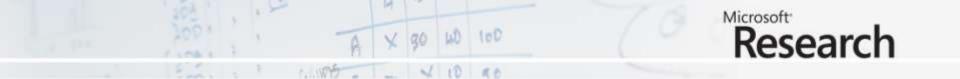


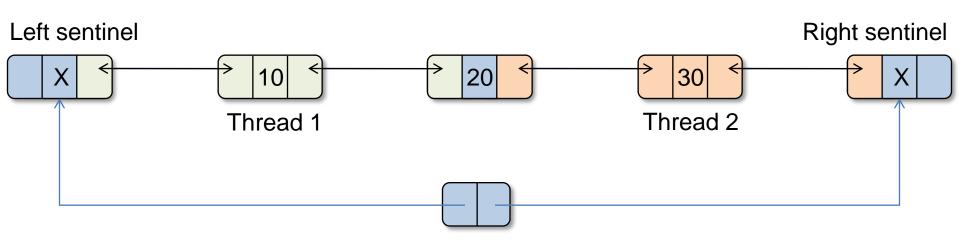
Making sense of transactional memory

Tim Harris (MSR Cambridge)

Based on joint work with colleagues at MSR Cambridge, MSR Mountain View, MSR Redmond, the Parallel Computing Platform group, Barcelona Supercomputing Centre, and the University of Cambridge Computer Lab



Example: double-ended queue



- Support push/pop on both ends
- Allow concurrency where possible
- Avoid deadlock

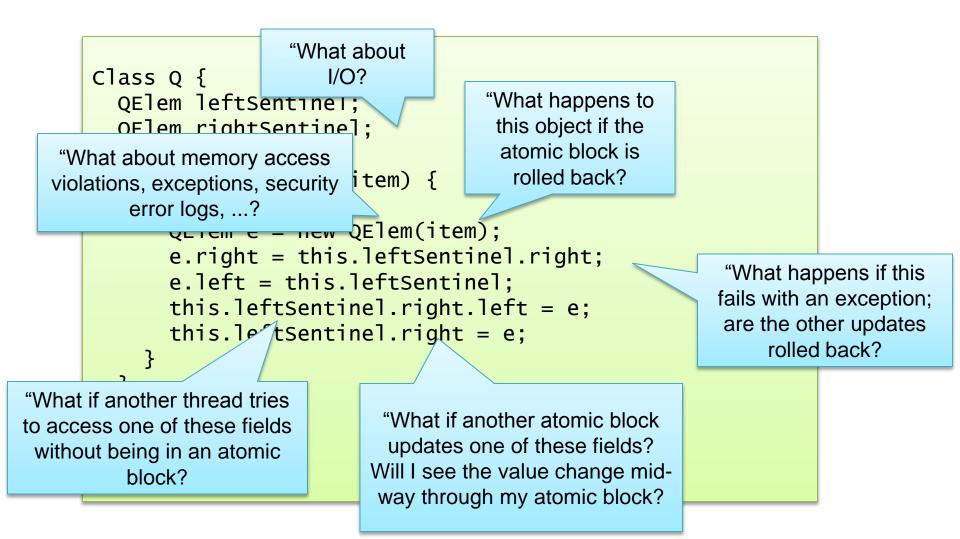


Implementing this: atomic blocks

```
Class Q {
  QElem leftSentinel;
  QElem rightSentinel;
  void pushLeft(int item) {
    atomic {
      QElem e = new QElem(item);
      e.right = this.leftSentinel.right;
      e.left = this.leftSentinel;
      this.leftSentinel.right.left = e;
      this.leftSentinel.right = e;
    }
  }
}
```

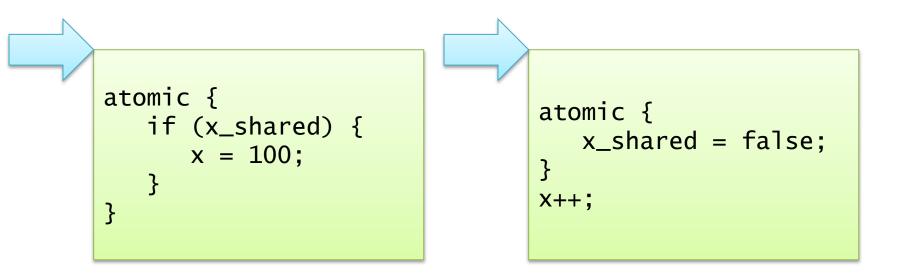


Design questions

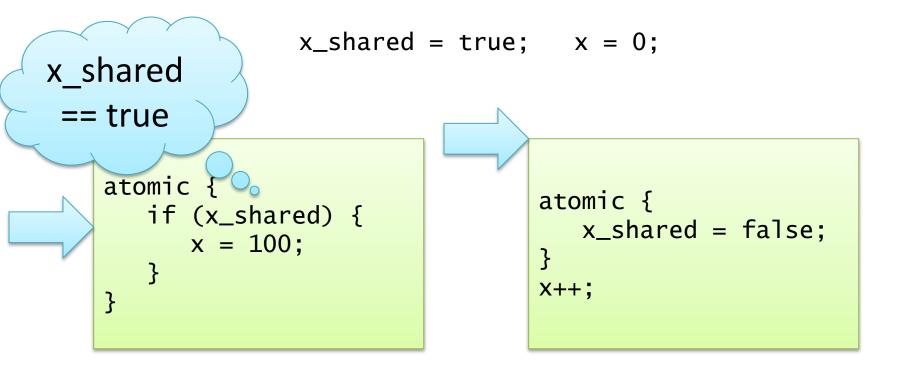




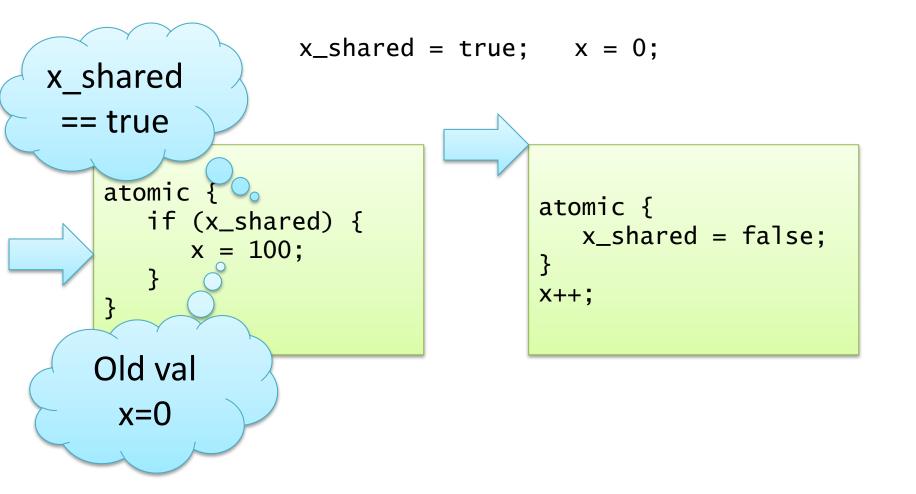
 $x_shared = true; x = 0;$



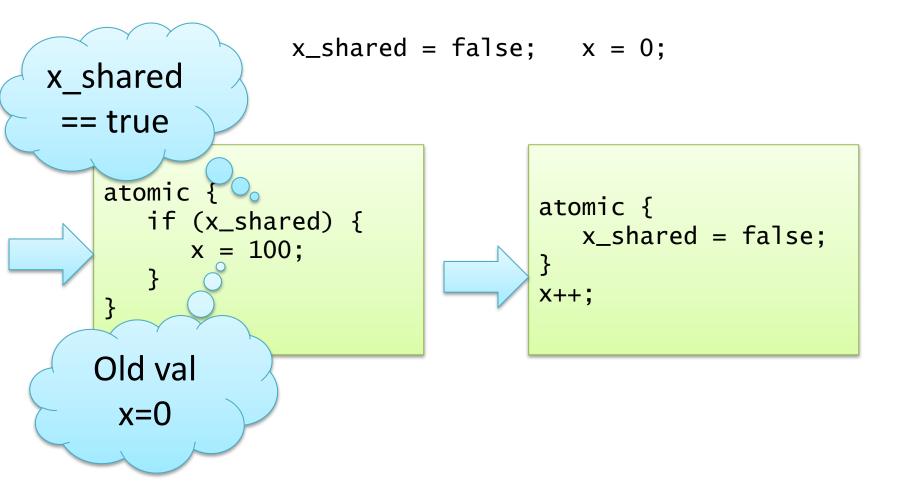




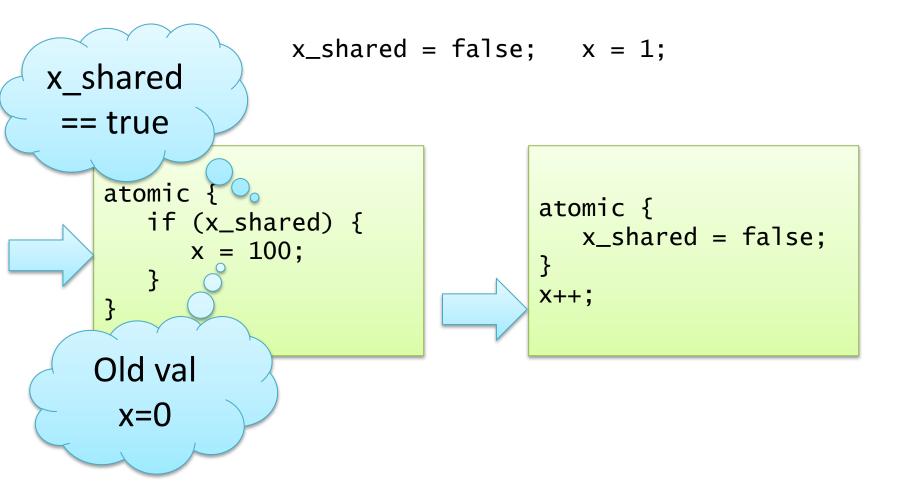




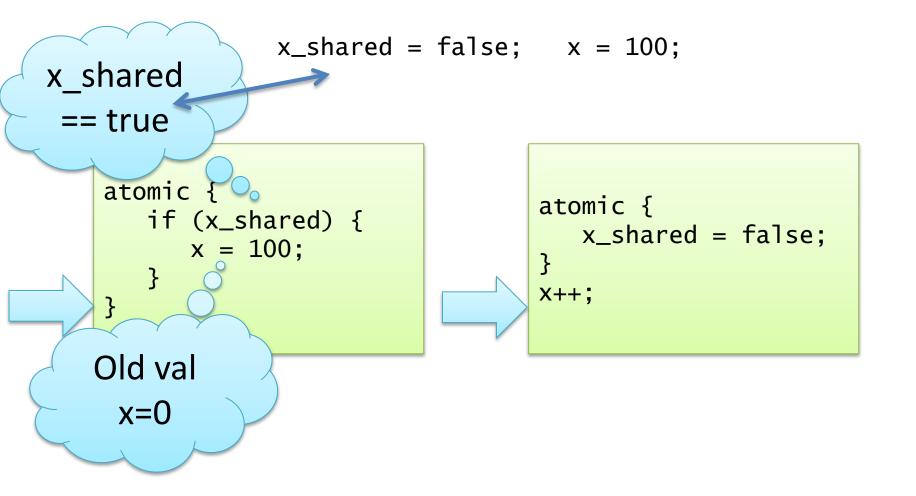




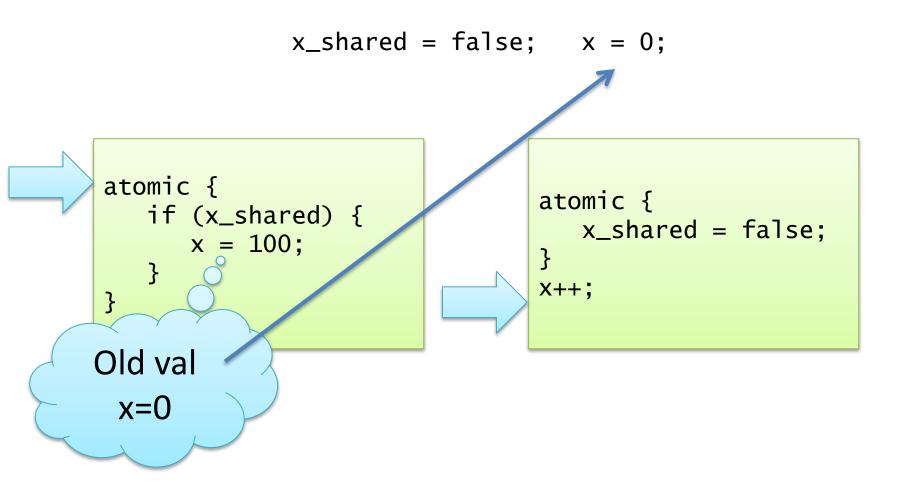






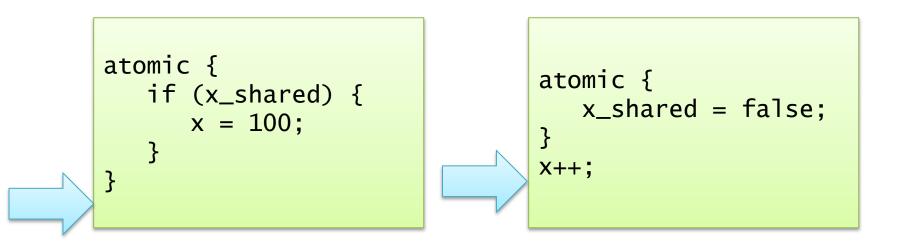






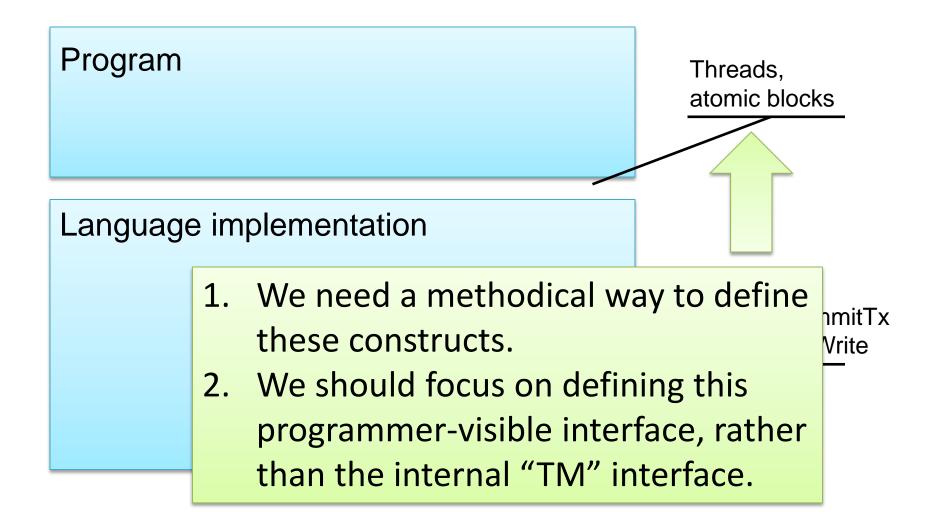


 $x_shared = false; x = 0;$



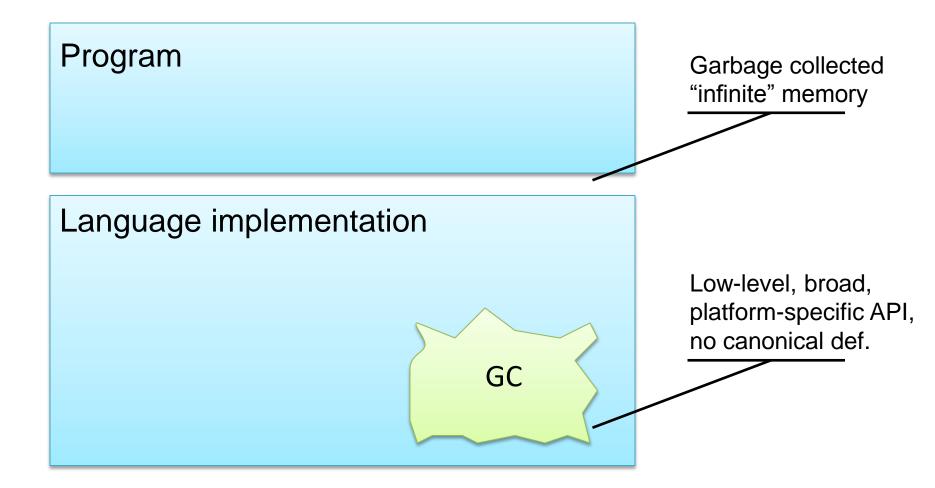


The main argument





An analogy





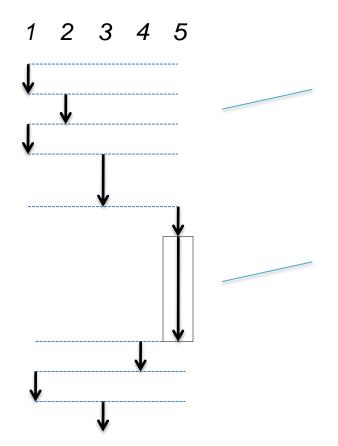
Defining "atomic", not "TM"

Implementing atomic over TM

Current performance



Strong semantics: a simple interleaved model

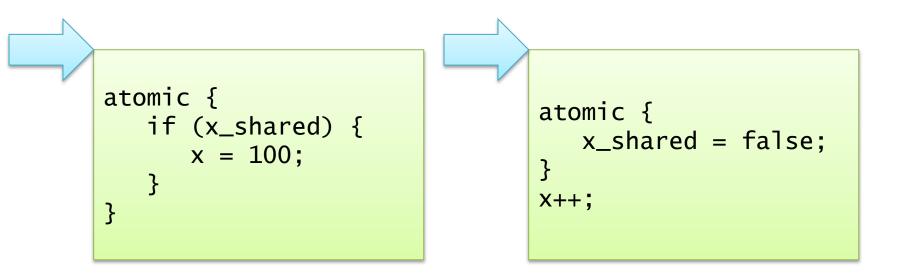


Sequential interleaving of operations by threads. No program transformations (optimization, weak memory, etc.)

Thread 5 enters an atomic block: prohibits the interleaving of operations from other threads



 $x_shared = true; x = 0;$



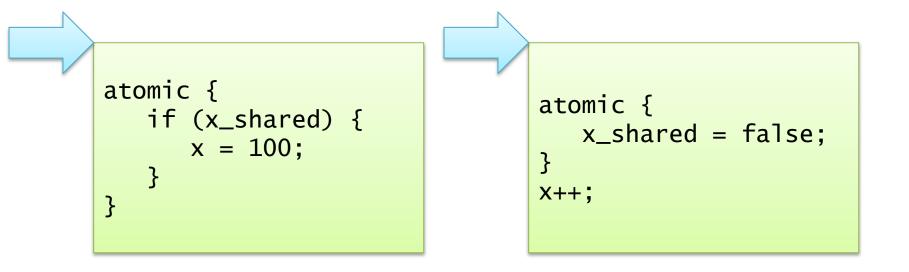


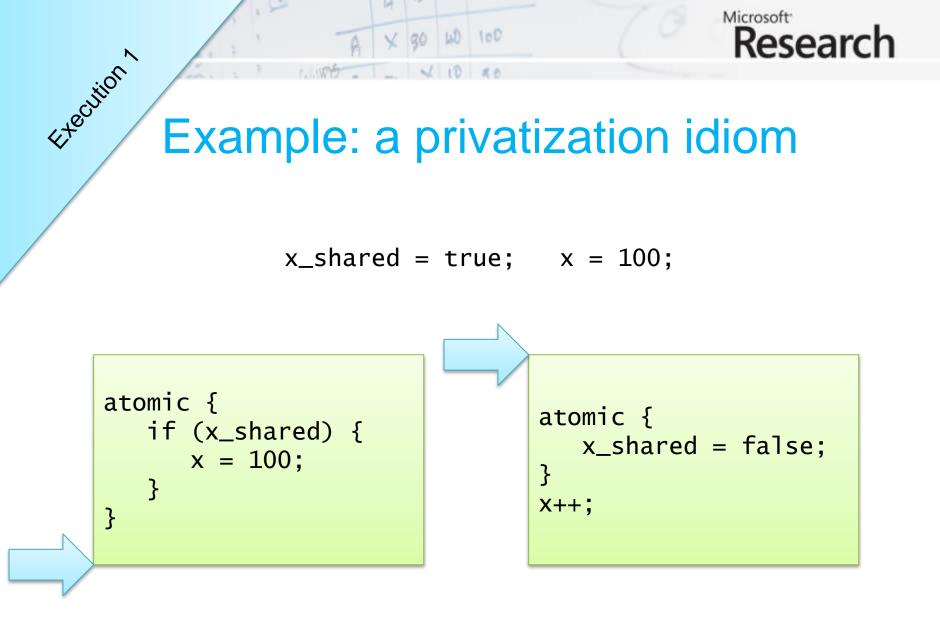
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Microsoft^{*}

Research

 $x_shared = true; x = 0;$





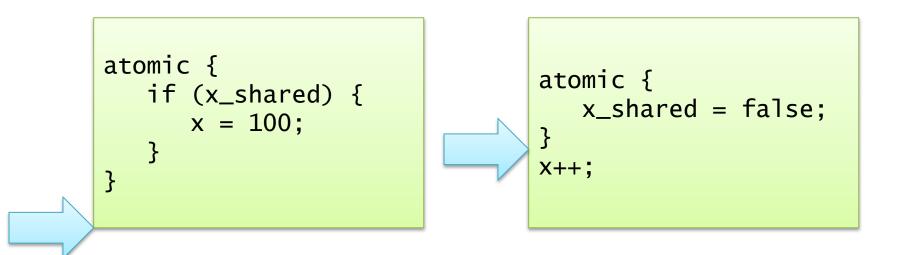
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Etection

Microsoft^{*}

Research

 $x_shared = false; x = 100;$



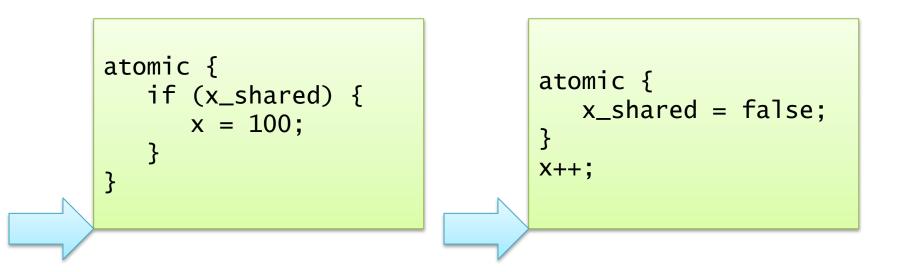
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Etection

Microsoft^{*}

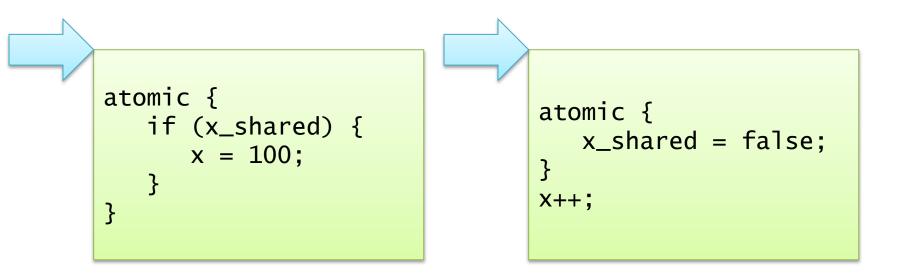
Research

 $x_shared = false; x = 101;$





 $x_shared = true; x = 0;$



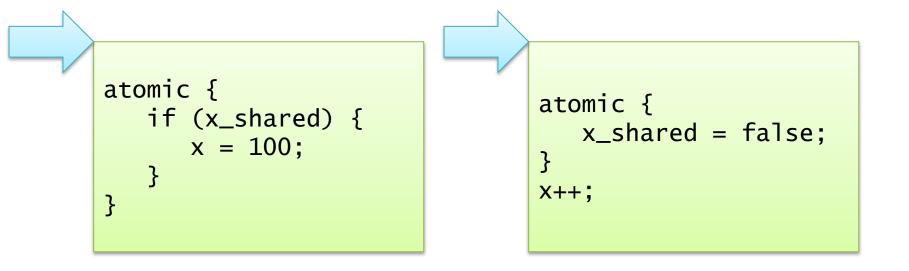


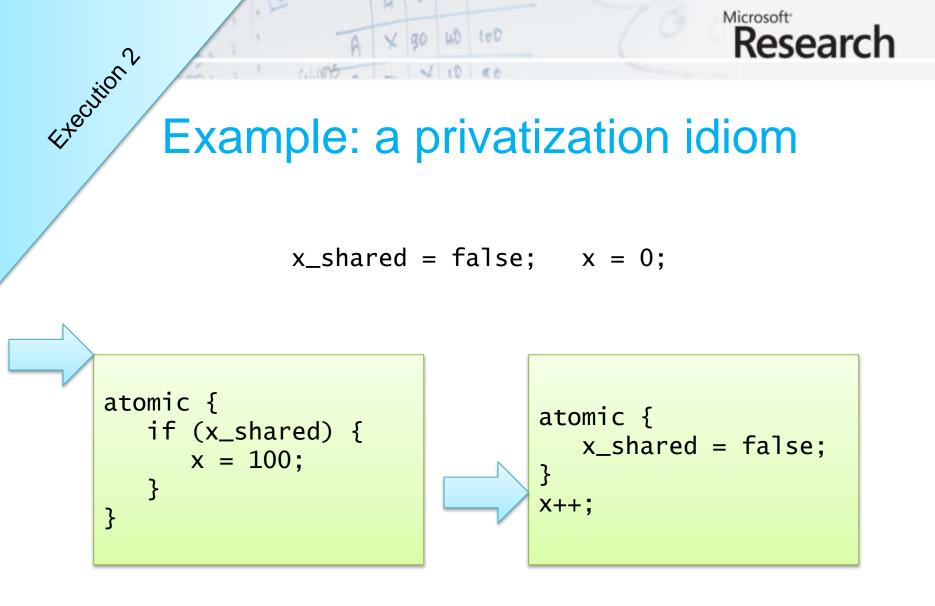
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Microsoft^{*}

Research

 $x_shared = true; x = 0;$





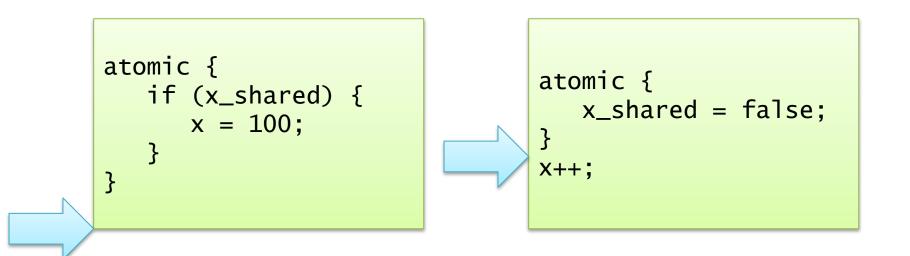
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Etection 2

Microsoft^{*}

Research

 $x_shared = false; x = 0;$



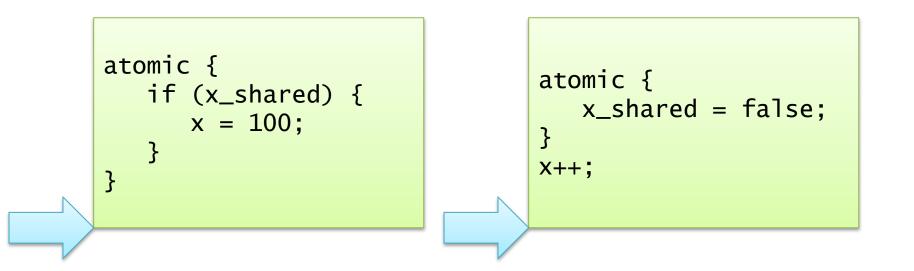
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Etection 2

Microsoft^{*}

Research

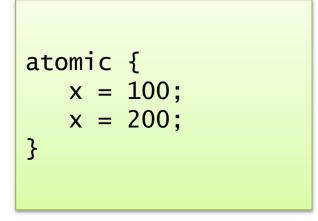
 $x_shared = false; x = 1;$



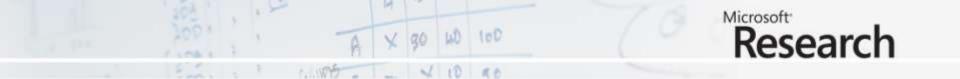


Pragmatically, do we care about...

x = 0;



temp = x; Console.WriteLine(temp);

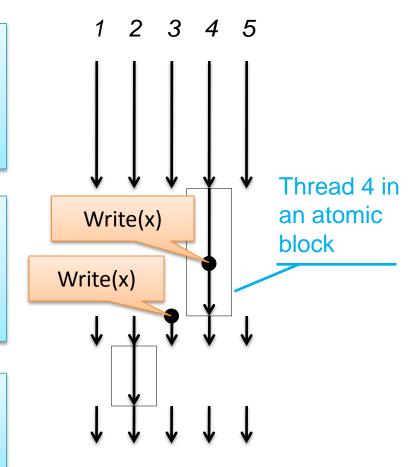


How: strong semantics for race-free programs

Strong semantics: simple interleaved model of multithreaded execution

Data race: concurrent accesses to the same location, at least one a write

Race-free: no data races (under strong semantics)





Hiding TM from programmers

Strong semantics

atomic, retry, what, ideally, should these constructs do?

Programming discipline(s)

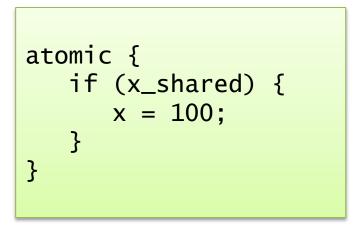
What does it mean for a program to use the constructs correctly?

Low-level semantics & actual implementations

Transactions, lock inference, optimistic concurrency, program transformations, weak memory models, ...



Correctly synchronized: no concurrent access to "x" under strong semantics

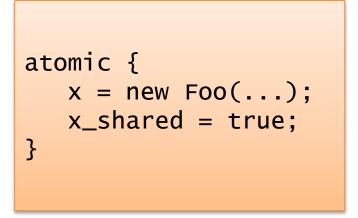




Example: a "racy" publication idiom

Not correctly synchronized: race on "x_shared" under strong semantics

x_shared = false; x = null;



if (x_shared) { // Use x }



What about...

- ...I/O?
- ...volatile fields?
- ...locks inside/outside atomic blocks?
- ...condition variables?

Methodical approach: what happens under the simple, interleaved model? 1. Ideally, what does it do? 2. Which uses are race-free?



What about I/O?

```
atomic {
   Console.WriteLine("What is your name?");
   x = Console.ReadLine();
   Console.WriteLine("Hello " + x);
}
```

The entire write-read-write sequence should run (as if) without interleaving with other threads



What about C#/Java volatile fields?

volatile int x, y = 0;

atomic {
x = 5;
y = 10;
x = 20;
}
}

r1 = x;
r2 = y;
r3 = x;

r1=20, r2=10, r3=20 r1=0, r2=10, r3=20 r1=0, r2=0, r3=20 r1=0, r2=0, r3=0



What about locks?

Correctly synchronized: both threads would need "obj1" to access "x"

```
atomic {
   lock(obj1);
   x = 42;
   unlock(obj1);
}
```

lock(obj1); x = 42; unlock(obj1);



What about locks?

Not correctly synchronized: no consistent synchronization

lock(obj1); x = 42; unlock(obj1);



What about condition variables?

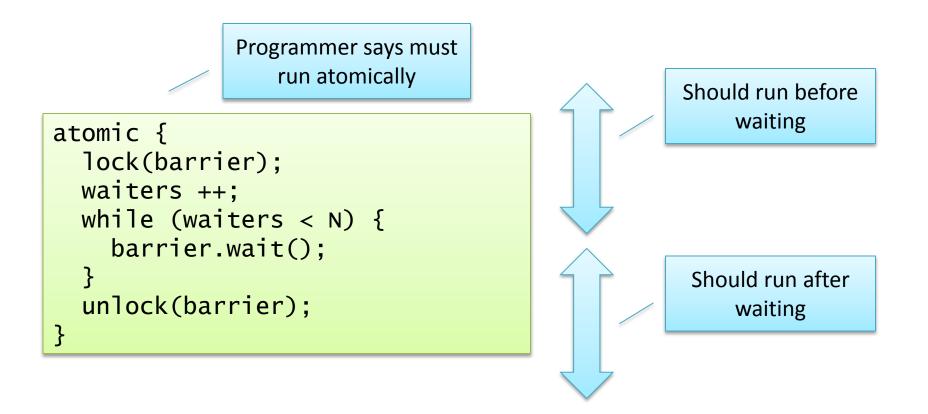
Correctly synchronized: ...and works OK in this example

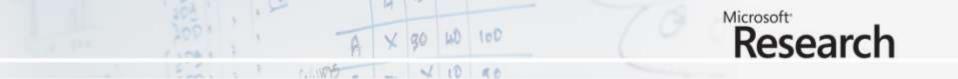
```
atomic {
   lock(buffer);
   while (!full) buffer.wait();
   full = true;
   ....
   unlock(buffer);
}
```

A X 90 40 100 Microsoft Research

What about condition variables?

Correctly synchronized: ...but program doesn't work in this example





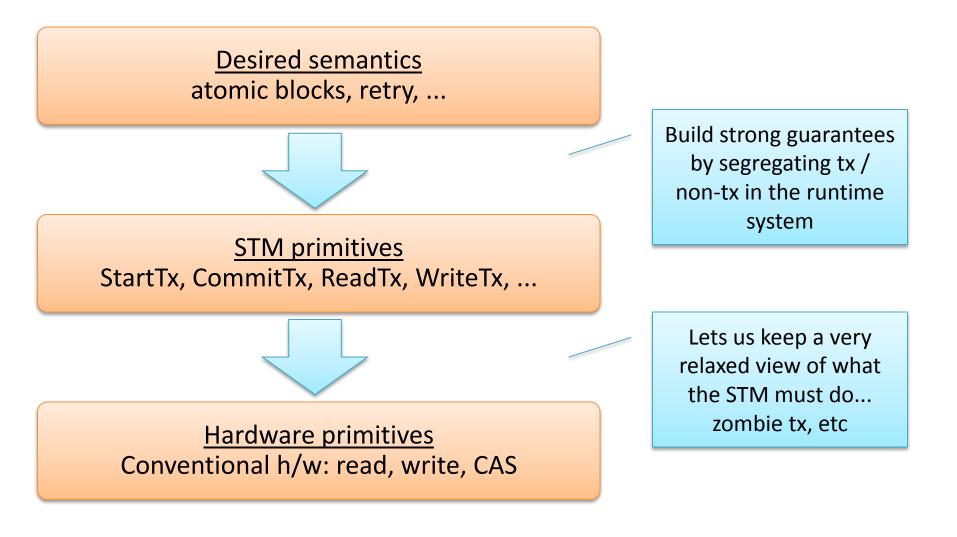
Defining "atomic", not "TM"

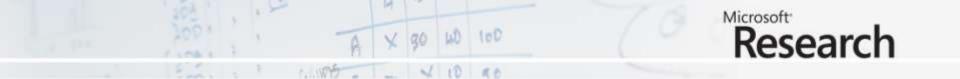
Implementing atomic over TM

Current performance

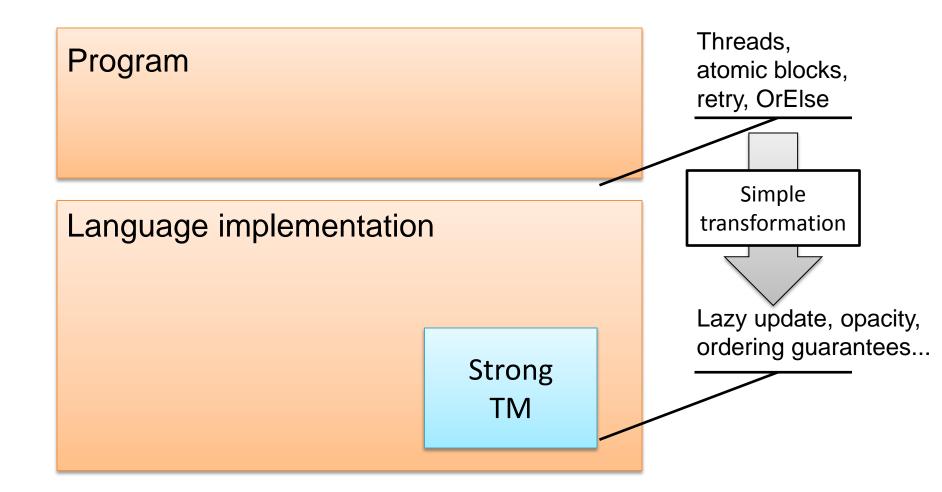


Division of responsibility



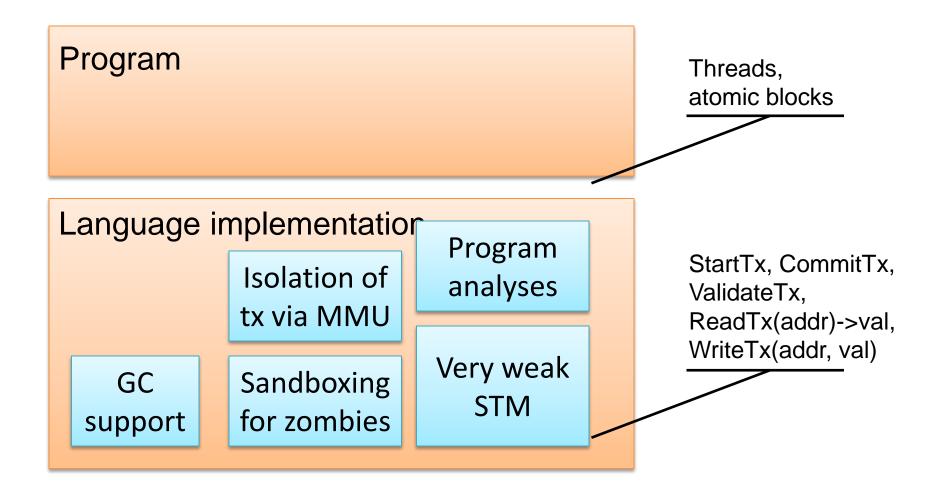


Implementation 1: "classical" atomic blocks on TM



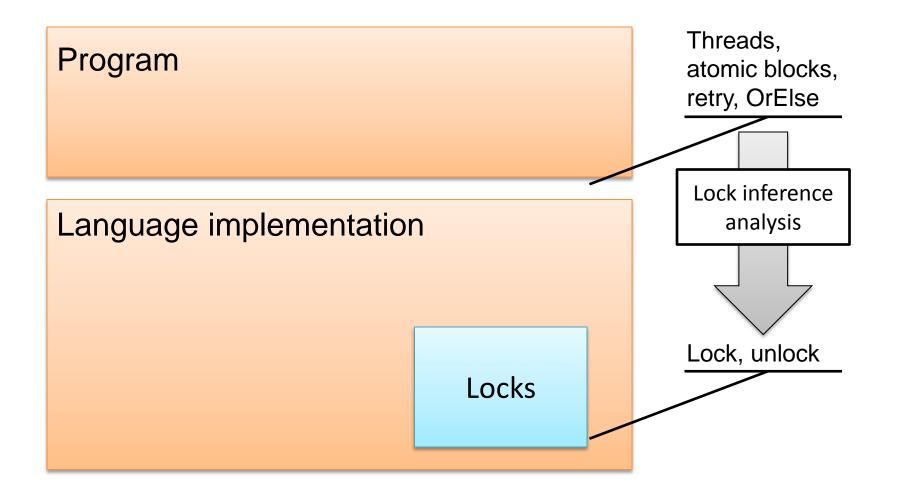


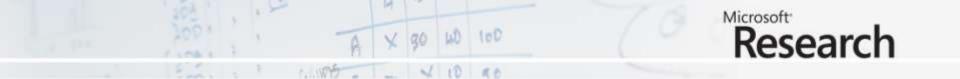
Implementation 2: very weak TM





Implementation 3: lock inference





- Prohibit
- Directly execute over
- Use irrevocable execution
- Integrate it with TM

Normal mutable state in STM-Haskell

"Dangerous" feature combinations, e.g, condition variables inside atomic blocks



- Prohibit
- Directly execute over TM
- Use irrevocable exec
- Integrate it with TM

e.g., an "ordinary" library abstraction used in an atomic block

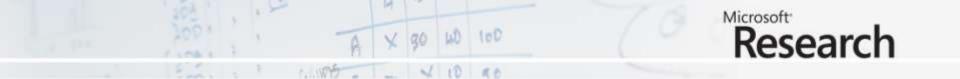
Is this possible? Will it scale well? Will this be correctly synchronized?



- Prohibit
- Directly execute over TM
- Use irrevocable execution
- Integrate it with TM

Prevent roll-back, ensure the transaction wins all conflicts.

Fall-back case for I/O operations. Use for rare cases, e.g., class initializers



- Prohibit
- Directly execute over TM
- Use irrevocable execution
- Integrate it with TM

Provide conflict detection, recovery, etc, e.g. via 2-phase commit

Low-level integration of GC, memory management, etc.



Defining "atomic", not "TM"

Implementing atomic over TM

Current performance

Performance figures depend on...

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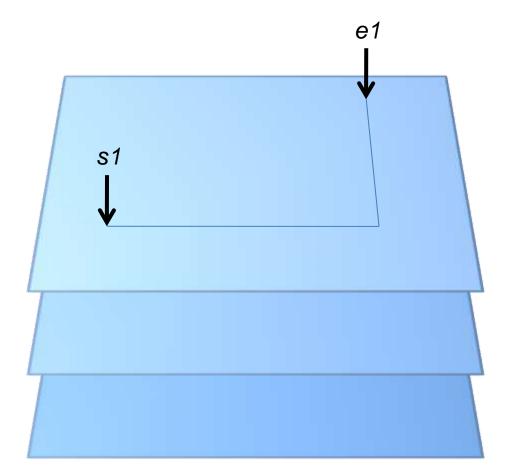
Microsoft^{*}

Research

- Workload : What do the atomic blocks do? How long is spent inside them?
- Baseline implementation: Mature existing compiler, or prototype?
- Intended semantics: Support static separation? Violation freedom (TDRF)?
- STM implementation: In-place updates, deferred updates, eager/lazy conflict detection, visible/invisible readers?
- STM-specific optimizations: e.g. to remove or downgrade redundant TM operations
- Integration: e.g. dynamically between the GC and the STM, or inlining of STM functions during compilation
- Implementation effort: low-level perf tweaks, tuning, etc.
- Hardware: e.g. performance of CAS and memory system



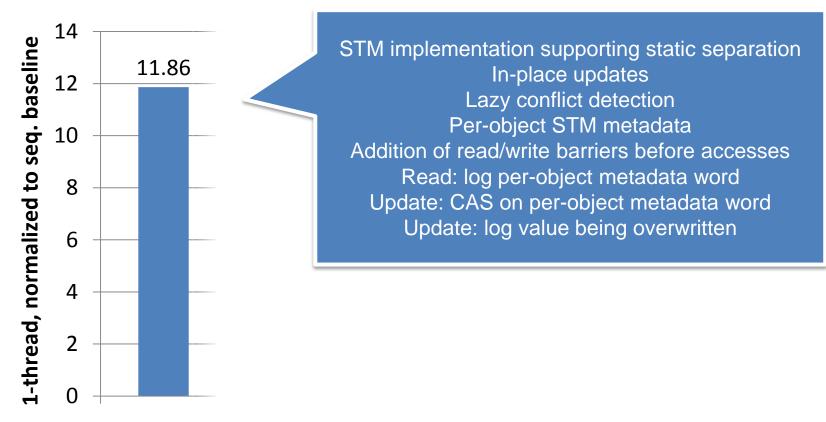
Labyrinth



- STAMP v0.9.10
- 256x256x3 grid
- Routing 256 paths
- Almost all execution inside atomic blocks
- Atomic blocks can attempt 100K+ updates
- C# version derived from original C
- Compiled using Bartok, whole program mode, C# -> x86 (~80% perf of original C with VS2008)
- Overhead results with Core2 Duo running Windows Vista

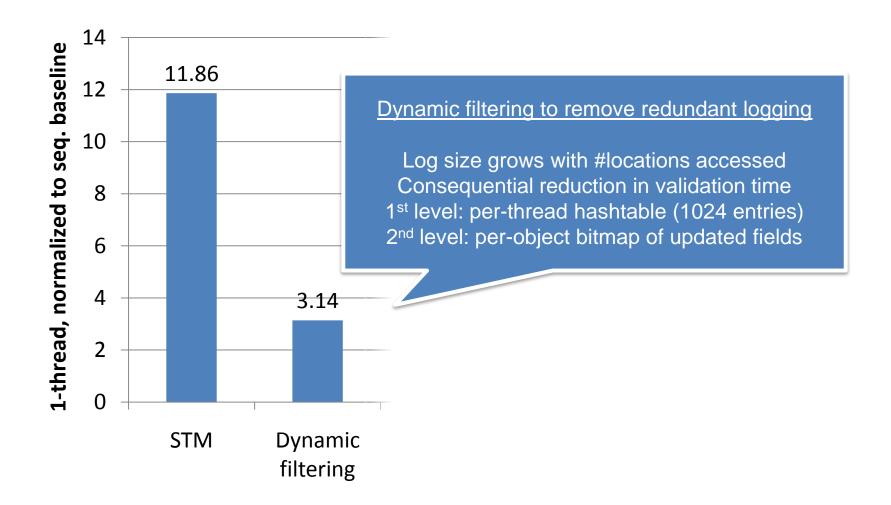
"STAMP: Stanford Transactional Applications for Multi-Processing" Chi Cao Minh, JaeWoong Chung, Christos Kozyrakis, Kunle Olukotun, IISWC 2008



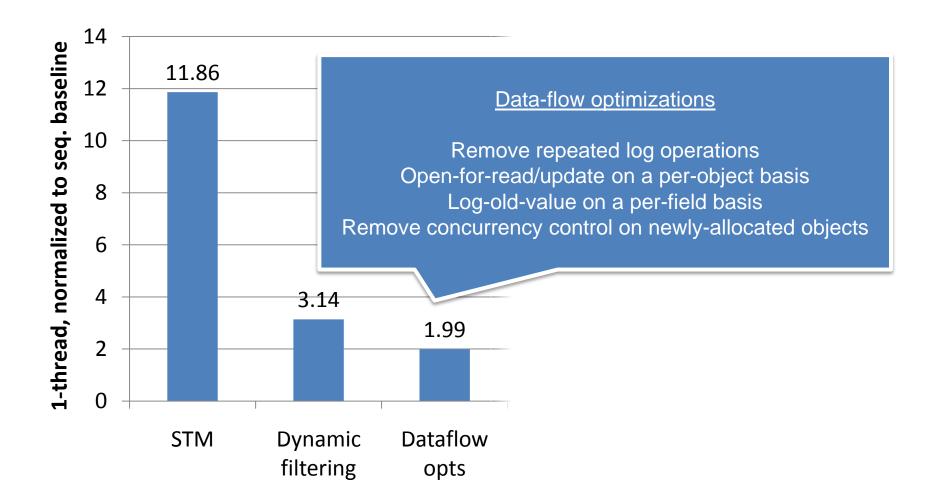


STM

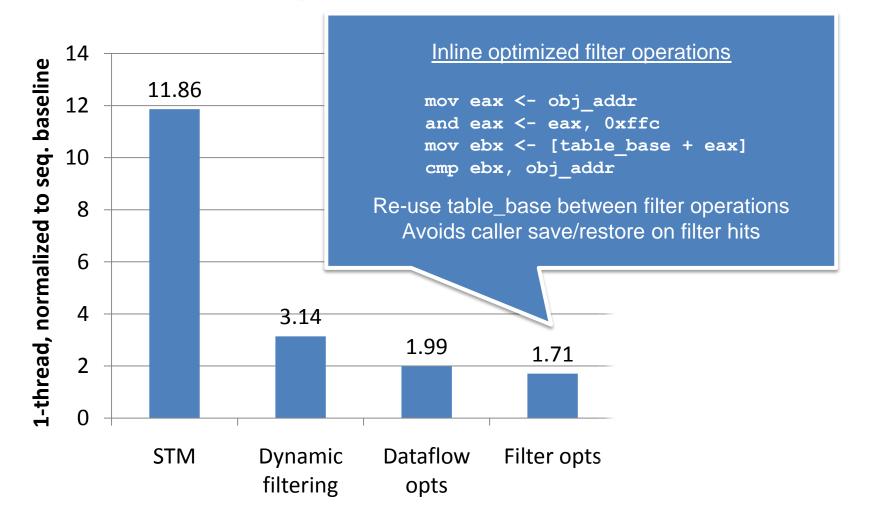




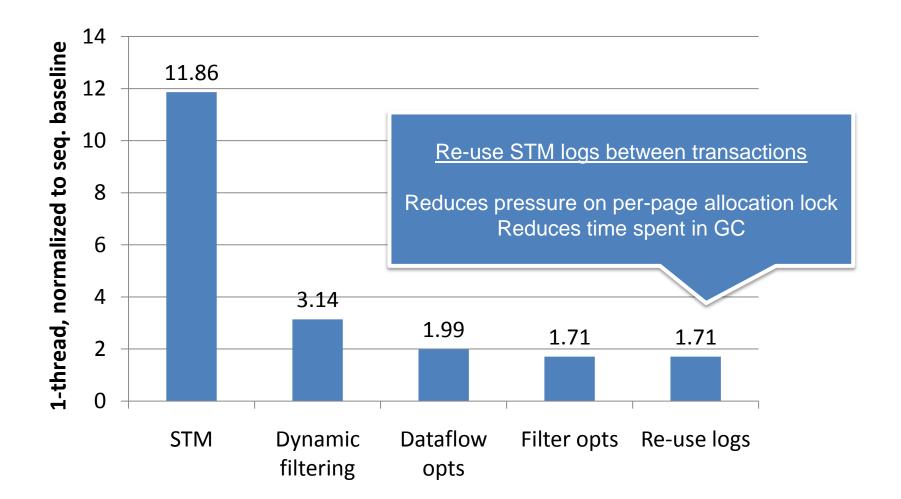






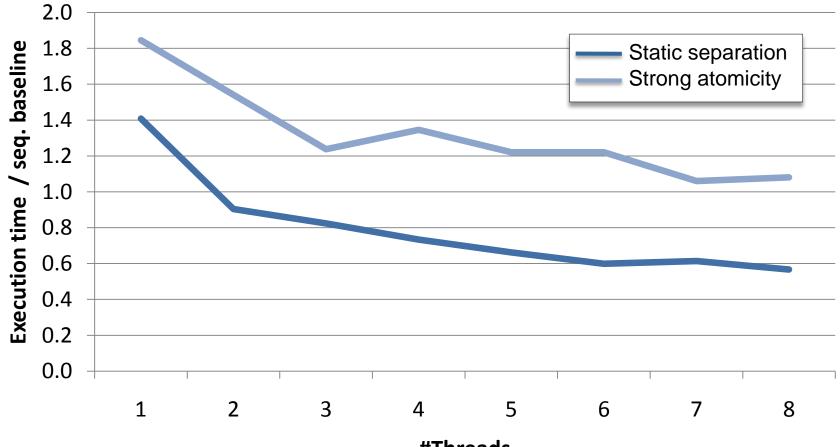








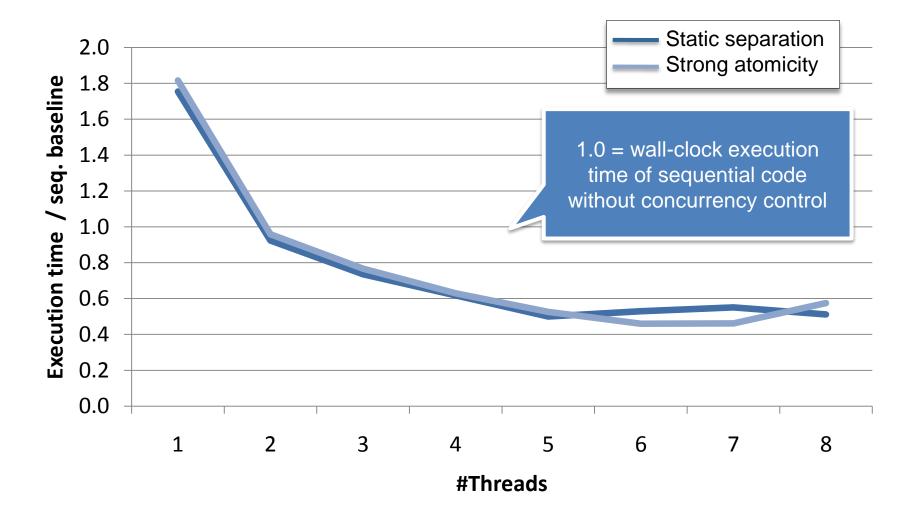
Scaling – Genome



#Threads



Scaling – Labyrinth





Making sense of TM

- Focus on the interface between the language and the programmer
 - Talk about atomicity, not TM
 - Permit a range of tx and non-tx implementations
- Define idealized "strong semantics" for the language (c.f. sequential consistency)
- Define what it means for a program to be "correctly synchronized" under these semantics
- Treat complicated cases methodically (I/O, locking, etc)