

1DT109 Accelerating Systems with Programmable Logic Components

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Key outcomes

- A holistic knowledge on FPGA design flow (of accelerator)
 - RTL modeling, System-level modeling, Verification, Implementation (using FPGA)
- Accelerator design space exploration
 - SW/HLS/RTL
- Cutting-edge accelerator architectures
 - Why they are good. The story behind the scene.

Learning goals

1. RTL level modeling using Verilog
 - Exceptionally synthesizable HDL code
 2. Popular accelerator architectures
 3. Build your own accelerator with Verilog
 - Compare it with other approaches
 4. Implement your design using FPGA
 - What is the magic of an FPGA tool?
 5. Verification, system-level modeling
- All lectures will be given via Zoom

Get yourself
ready as an
FPGA design
engineer/
researcher.

Components of the course

Recap: basics of digital design

Verilog
(Synthesisable design)

High-level synthesis

Acceleration
(Cutting-edge accelerator architecture)

Testing verification

System-level modelling with SystemC

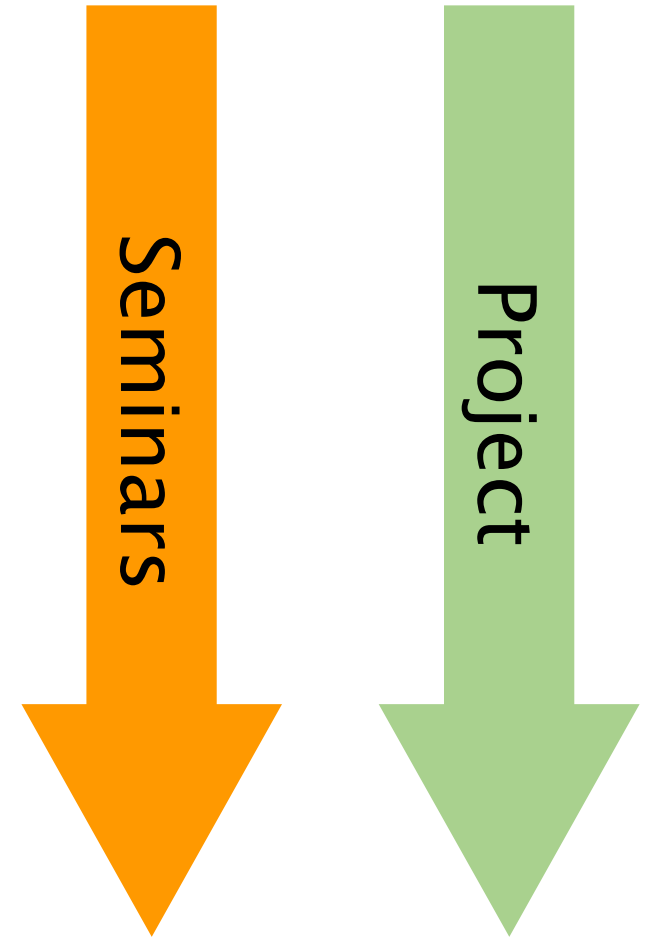
Lab 1

Lab 2

Lab 3

Seminars

Project



Lectures

- Digital Design
- Verilog
- High-level synthesis
- Hardware accelerators
- FPGAs, Buses, PS-PL interface
- Testing and Verification
- System-level modelling with SystemC (new this year!)
 - Is based on C++
 - Is heavily used in industry, e.g. Ericsson

Labs

- Done using simulators, no hardware
- Groups of two people

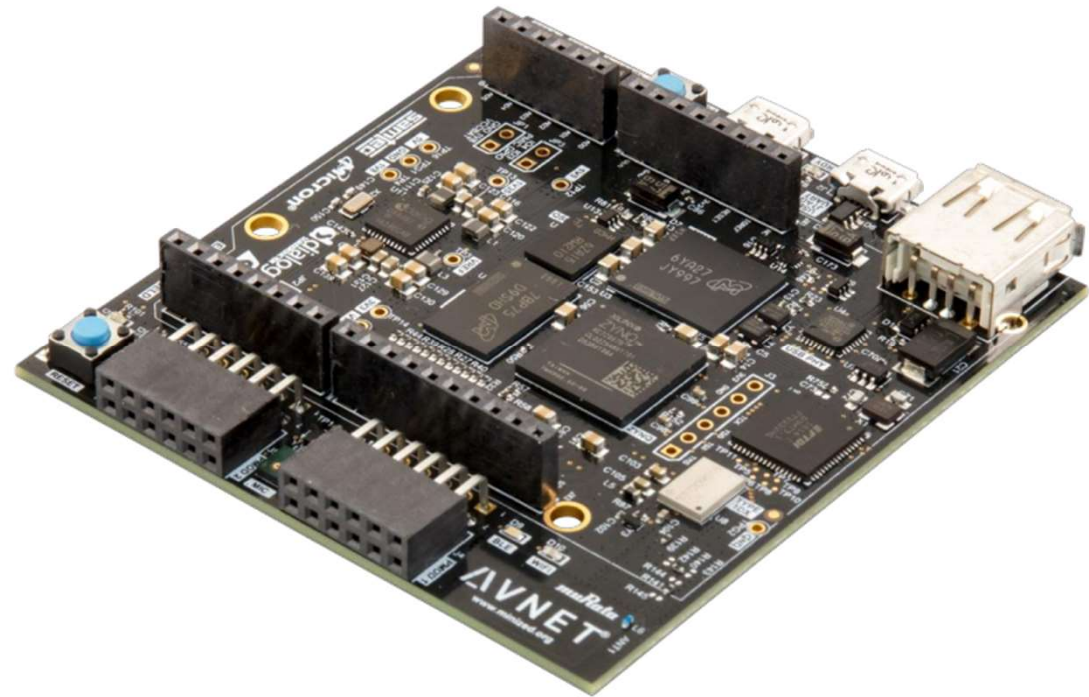
- Lab 1: Interfacing an external keyboard
- Lab 2: Accelerating a computation, the AXI bus
- Lab 3: Testing a Verilog implementation
- (Opt) Lab 4: Connecting accelerators using SystemC

Project

- Groups of two people
- Complete picture:
Acceleration of an actual application/algorithm
- Performance evaluation:
 - Software
 - Hand-written Verilog RTL
 - High-level synthesis

MiniZed boards

- Xilinx Zynq XC7Z007S SoC (Zynq 7000)
- Single ARM Cortex A9 core running Linux
- 512MB DDR
- Goal is to provide one board for each student



Reading Assignments + Seminars

- Research papers on acceleration
- Book chapters on acceleration
- Presented either individually, or in groups of two (you can choose)
- Each presentation ~25min (via Zoom), with a short discussion afterwards