HiPEAC = High-Performance Embedded Architecture and Compilers
-- an EU FP7 Network of Excellence --

HiPEAC Roadmaps

2008 2009 2011

http://www.hipeac.net/roadmap
(these slides are a short version of the HiPEAC presentation)

Part of the HiPEAC roadmap is required reading for AVDARK
You will find it and other required reading in the "Extra course papers" directory.
As specified in the "Reading instructions":
• page 2-33 required reading
• page 34-40 read-through (RT)
**Trends influencing Computing Systems**

**Application Pull**
- Data Deluge
- Intelligent Processing
- Ubiquitous Communication

**Business Trends**
- Convergence
- Specialization
- Post-PC Devices

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**Data Deluge**

The "data deluge" gap

Source: "The Landscape of Parallel Computing Research: A View from Berkeley" Krste Asanovic et al.

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**Growth of data storage in Exabytes**


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**Ubiquitous computing in a connected world**

- Sensory swarm, actuators and real world data
- Smart house cities, …
- Mobile access

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**Trends influencing Computing Systems**

**Application Pull**
- Data Deluge
- Intelligent Processing
- Ubiquitous Communication

**Business Trends**
- Convergence/standards
- Specialization
- Post-PC Devices
Convergence

- Business models
- Standard(s)
- Interoperability
- ...

IP, Internet

Broadcast

Telecom

Post-PC devices

Ubiquitous access

PC Market

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<td>100</td>
<td>12,650</td>
<td>100</td>
<td>-18.9</td>
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Note: Data includes only PC units not notebook/PC tablets are excluded. Source: Gartner (August 2011)

Computing Systems: Drivers

Application pull

Business trends

Technological trends influencing Computing Systems

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Opportunities</th>
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<tbody>
<tr>
<td>Frequency Limits</td>
<td>CMOS Phonotic</td>
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<td>Power Limits</td>
<td>Non-volatile memories</td>
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<td>Dark Silicon</td>
<td>3D Stacking</td>
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<tr>
<td></td>
<td>New paradigms</td>
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Technological constraints

We are at a turning point

Continuation of Moore’s Law

Power limits

Dark silicon

Moore’s law: increase in transistor density

Data from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic

Limited frequency increase ⇒ more cores

Limitation by power density and dissipation

2009: GP CPU = 130 W (45 nm)
2009: Consumer SoC = 10W
2009: Mobile SoC = 1 W

Data from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic

Dark Silicon

Source: Kristzán Flautner “From niche to mainstream: can critical systems make the transition?”

Specialization leads to more efficiency

Source: Bill Dally, “To Exascale and Beyond”

www.nvidia.com/content/PDFor_2010/theater/Dally_SC10.pdf
Locality and communications management

- In 22 nm, swapping 1 bit in a transistor has an energy cost:
  \[ \approx 1 \text{ attojoule} \left(10^{-18} \text{ J}\right) \]
- Moving a 1-bit data on the silicon cost:
  \[ \approx 1 \text{ picojoule/mm} \left(10^{-12} \text{ J/mm}\right) \]
- Moving a data \(10^9\) per second (1 GHz) in silicon has a cost:
  \[ 1 \text{ pJ/mm} \times 10^9 \text{ s}^{-1} = \approx 1 \text{ milliwatt/mm} \]
- 64 bit bus @ 1 GHz: \(\approx 64\) milliwatts/mm (with 100% activity)
- For 1 cm of 64 bit bus @ 1 GHz: \(0.64\) W/cm

- On modern chips, there are about several km of wires on chip, even with low toggle rate, this leads to several W/cm²

Technological trends influencing Computing Systems

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Optical interconnects

CMOS photonic is the integration of a photonic layer with an electronic circuit.

Advantages of CMOS photonic area:
- Use of standard tools and foundry, wafer scale co-integration
- Lower energy (~100 fJ/bit), (wire: ~1 pJ/mm)
- High bandwidth (10 Gbps), Low latency (~10 ps/mm)

Example: Memristive Devices Principle

\[ v = R(x,t)i \]
\[ \frac{dx}{dt} = f(x,i) \]

Non-volatile memories....

Example: Memristive Devices Principle

Source: CEA, Ahmed Jerraya

Source: CEA, C. Gamrat
3D stacking

Multiple integration with 3D stacking...

Source: STMicroelectronics & CEA

Technology also drives us to think differently...

- Stochastic computing
- Biologically inspired computing
- Organic Computing
- Autonomous computing, Self-

- Smart spaces (smart house, town, building, rooms,...)
- Intelligent dust (smart sensors)
- 3D stacking
- Photonic interconnect
- Non-volatile memories
- Molecular computing
- More-than-Moore
- Spintronics
- Chemical computing
- Biologically inspired cells
- Memristors
- Also silicon based!

Core Computing Systems Challenges

<table>
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<tr>
<th>Efficiency</th>
<th>Complexity</th>
<th>Dependability</th>
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<tr>
<td>Power</td>
<td>Parallelism</td>
<td>Reliability</td>
</tr>
<tr>
<td>Performance</td>
<td>Heterogeneity</td>
<td>Privacy</td>
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Improving efficiency

- Multiple performance metrics
- Power defines performance
- Communication defines performance
- Heterogeneity and accelerators to the rescue

Managing complexity

- The reign of legacy code
- Parallelism seems to be too complex for humans
- Hardware complexity

(4G is 500x more complex than 2G)
Improving dependability

• Worst case design is not an option anymore
• Systems must be built from unreliable components
• Safety and security!

Derived HiPEAC Research Objectives

• Cost-effective software for heterogeneous multicores
• Cross-component/cross-layer optimization for design integration
• Next-generation processor cores

Cost-effective software for heterogeneous multicores

Frequency limit → parallelism
Energy efficiency → heterogeneity
Ease of programming
Exiting new opportunities are ahead of us!