IP-based design is inevitable, taking into account the complexities of today's electronic designs. One such IP core that plays an important role in IP-based designs is the microprocessor core. Soft processor cores are delivered as RTL code and provide high flexibility for users. This work aims at improving an existing soft microprocessor core optimized for Xilinx Virtex-II FPGA, which runs at a very high clock frequency of around 300 MHz, whereas most processor cores released by FPGA vendors run at about 200 MHz. Improvement includes design and implementation of instruction and data caches. Mechanisms to allow non-cacheable memory access are also implemented. Interrupt support and exception handling is added as well, preparing the microprocessor core to host MMU-less operating systems such as uClinux, and full Linux provided that MMU is also added to the processor core. Thorough verification of the added modules is heavily emphasized in this work. Maintaining core clock frequency at its maximum has been the main concern through all the design and implementation steps.