Publications from the Uppsala Architecture Research Team (UART)

Most of them are also available electronically from UART's Web page:

`http://www.it.uu.se/research/group/uart/`.

References

[1] Albertsson, L. Simulation-Based Debugging of Soft Real-Time Applications. In *Proceedings of the Real-Time Application Symposium* (May 2001).

[2] Albertsson, L. Temporal Debugging and Profiling of Multimedia Applications. In *Proceedings of Multimedia Computing and Networking 2002* (San José, California, USA, Jan. 2002).

[3] Albertsson, L., and Magnusson, P. S. Simulation-Based Temporal Debugging of Linux. In *Proceedings of the 2nd Real-Time Linux Workshop* (Lake Buena Vista, Florida, USA, Nov. 2000).

[4] Albertsson, L., and Magnusson, P. S. Using Complete System Simulation for Temporal Debugging of General Purpose Operating Systems and Workloads. In *Proceedings of the 8th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS 2000)* (San Francisco, California, USA, Aug. 2000).

[5] Berg, E. *Methods for Run Time Analysis of Data Locality.* Licentiate thesis, Department of Information Technology, Uppsala University, Dec. 2003.

[6] Berg, E. *Efficient and Flexible Characterization of Data Locality through Native Execution Sampling.* PhD thesis, Department of Information Technology, Uppsala University, Nov. 2005.

[7] Berg, E., and Hagersten, E. SIP: Performance Tuning through Source Code Interdependence. In *Proceedings of the 8th International Euro-Par Conference (Euro-Par 2002)* (Paderborn, Germany, Aug. 2002), pp. 177–186.

[8] Berg, E., and Hagersten, E. Low-Overhead Spatial and Temporal Data Locality Analysis. Tech. Rep. 2003-057, Department of Information Technology, Uppsala University, Nov. 2003.

[9] Berg, E., and Hagersten, E. StatCache: A Probabilistic Approach to Efficient and Accurate Data Locality Analysis. Tech. Rep. 2003-058, Department of Information Technology, Uppsala University, Nov. 2003.

[10] Berg, E., and Hagersten, E. StatCache: A Probabilistic Approach to Efficient and Accurate Data Locality Analysis. In *Proceedings of the 2004 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2004)* (Austin, Texas, USA, Mar. 2004).

[11] Berg, E., and Hagersten, E. Fast Data-Locality Profiling of Native Execution. In *Proceedings of ACM SIGMETRICS 2005* (Banff, Canada, June 2005).

[12] Berg, E., Zeffer, H., and Hagersten, E. . In *Proceedings of the 2006 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2006)* (Austin, Texas, USA, Mar. 2006).

[13] Ekström, N. Improving DSZOOM's Run Time System. Master's thesis, School of Engineering, Uppsala University, Sweden, Jan. 2004.

[14] Grenholm, O. Simple and Efficient Instrumentation for the DSZOOM System. Master's thesis, School of Engineering, Uppsala University, Sweden, Dec. 2002.

[15] Grenholm, O., Radović, Z., and Hagersten, E. Latency-hiding and Optimizations of the DSZOOM Instrumentation System. Tech. Rep. 2003-029, Department of Information Technology, Uppsala University, May 2003.

[16] Hagersten, E., and Koster, M. WildFire: A Scalable Path for SMPs. In *Proceedings of the 5th International Symposium on High-Performance Computer Architeture (HPCA-5)* (Orlando, Florida, USA, Jan. 1999), pp. 172–181.

[17] Hagersten, E., and Papadopoulos, G. Scanning the DSM Technology. *Proceedings of the IEEE* (Mar. 1999).

[18] Holmgren, S., Rantakokko, J., Norden, M., and Wallin, D. Performance of PDE Solvers on a Self-Optimizing NUMA Architecture. *Parallel Algorithms and Applications 17*, 4 (2003), 285–299.

[19] Holmgren, S., and Wallin, D. Performance of a High-Accuracy PDE Solver on a Self Optimizing NUMA Architecture. In *Proceedings of the 7th International Euro-Par Conference (Euro-Par 2001)* (Manchester, UK, Aug. 2001).

[20] Karlsson, M. *Cache Memory Design Trade-offs for Current and Emerging Workloads*. Licentiate thesis, Department of Information Technology, Uppsala University, Sept. 2003.

[21] Karlsson, M., and Hagersten, E. Timestamp-Based Selective Cache Allocation. In *Proceedings of the Workshop on Memory Performance Issues, held in conjunction with the 28th International Symposium on Computer Architecture (ISCA28)* (Göteborg, Sweden, June 2001).

[22] Karlsson, M., Moore, K., Hagersten, E., and Wood, D. Memory Characterization of the ECperf Benchmark. In *Proceedings of the 2nd Annual Workshop on Memory Performance Issues (WMPI 2002), held in conjunction with the 29th International Symposium on Computer Architecture (ISCA29)* (Anchorage, Alaska, USA, May 2002).

[23] Karlsson, M., Moore, K., Hagersten, E., and Wood, D. Memory System Behavior of Java-Based Middleware. In *Proceedings of the 9th International Symposium on High-Performance Computer Architeture (HPCA-9)* (Anaheim, California, USA, Feb. 2003), pp. 217–228.

[24] Karlsson, M., Moore, K., Hagersten, E., and Wood, D. . In *Proceedings of the 2005 International Conference on Parallel Processing (ICPP-05)* (Oslo, Norway, June 2005).

[25] Löf, H., Radović, Z., and Hagersten, E. THROOM — Running POSIX Multithreaded Binaries on a Cluster. Tech. Rep. 2003-026, Department of Information Technology, Uppsala University, Apr. 2003.

[26] Löf, H., Radović, Z., and Hagersten, E. THROOM - Supporting POSIX Multithreaded Binaries on a Cluster. In *Proceedings of the 9th International Euro-Par Conference (Euro-Par 2003)* (Klagenfurt, Austria, Aug. 2003), pp. 760–769.

[27] Radović, Z. DSZOOM – Low Latency Software-Based Shared Memory. Master's thesis, School of Engineering, Uppsala University, Sweden, Dec. 2000.

[28] Radović, Z. *Efficient Synchronization and Coherence for Nonuniform Communication Architectures.* Licentiate thesis, Department of Information Technology, Uppsala University, Sept. 2003.

[29] Radovi'c, Z. *Software Techniques for Distributed Shared Memory.* PhD thesis, Department of Information Technology, Uppsala University, Nov. 2005.

[30] Radović, Z., and Hagersten, E. DSZOOM – Low Latency Software-Based Shared Memory. Tech. Rep. 2001:03, Parallel and Scientific Computing Institute (PSCI), Sweden, Apr. 2001.

[31] Radović, Z., and Hagersten, E. Implementing Low Latency Distributed Software-Based Shared Memory. In *Proceedings of the Workshop on Memory Performance Issues, held in conjunction with the 28th International Symposium on Computer Architecture (ISCA28)* (Göteborg, Sweden, June 2001).

[32] Radović, Z., and Hagersten, E. Removing the Overhead from Software-Based Shared Memory. In *Proceedings of Supercomputing 2001* (Denver, Colorado, USA, Nov. 2001).

[33] Radović, Z., and Hagersten, E. Efficient Synchronization for Non-Uniform Communication Architectures. In *Proceedings of Supercomputing 2002* (Baltimore, Maryland, USA, Nov. 2002).

[34] Radović, Z., and Hagersten, E. RH Lock: A Scalable Hierarchical Spin Lock. In *Proceedings of the 2nd Annual Workshop on Memory Performance Issues (WMPI 2002), held in conjunction with the 29th International Symposium on Computer Architecture (ISCA29)* (Anchorage, Alaska, USA, May 2002).

[35] Radović, Z., and Hagersten, E. Hierarchical Backoff Locks for Nonuniform Communication Architectures. In *Proceedings of the 9th International Symposium on High-Performance Computer Architeture (HPCA-9)* (Anaheim, California, USA, Feb. 2003), pp. 241–252.

[36] Selén, T. Reorganisation in the skewed-associative tlb. Tech. Rep. 2004-027, Department of Information Technology, Uppsala University, Sept. 2004. M.Sc. thesis.

[37] Spjuth, M. Refinement and Evaluation of the Elbow Cache. Master's thesis, School of Engineering, Uppsala University, Sweden, Apr. 2002.

[38] Spjuth, M., Karlsson, M., and Hagersten, E. The Elbow Cache: A Power-Efficient Alternative to Highly Associative Caches. Tech. Rep. 2003-046, Department of Information Technology, Uppsala University, Sept. 2003.

[39] Spjuth, M., Karlsson, M., and Hagersten, E. Low Power and Conflict Tolerant Cache Design. Tech. Rep. 2004-024, Department of Information Technology, Uppsala University, May 2004.

[40] Spjuth, M., Karlsson, M., and Hagersten, E. Skewed Caches from a Low-Power Perspective. In *Proceedings of Computing Frontiers* (Ischia, Italy, May 2005).

[41] Stenström, P., Hagersten, E., Lilja, D., Martonosi, M., and Venugopal, M. *Shared-Memory Multiprocessing: Current State and Future Directions*, vol. 53. Academic Press, 2000, ch. 1, pp. 2–46.

[42] Wallin, D. Performance of a High-Accuracy PDE Solver on a Self Optimizing NUMA Architecture. Master's thesis, School of Engineering, Uppsala University, Sweden, Feb. 2001.

[43] Wallin, D. *Exploiting Data Locality in Adaptive Architectures*. Licentiate thesis, Department of Information Technology, Uppsala University, Sept. 2003.

[44] Wallin, D., and Hagersten, E. Bundling: Reducing the Overhead of Multiprocessor Prefetchers. Tech. Rep. 2003-037, Department of Information Technology, Uppsala University, Aug. 2003.

[45] Wallin, D., and Hagersten, E. Miss Penalty Reduction Using Bundled Capacity Prefetching in Multiprocessors. In *Proceedings of the 17th International Parallel and Distributed Processing Symposium (IPDPS 2003)* (Nice, France, Apr. 2003).

[46] Wallin, D., and Hagersten, E. Bundling: Reducing the Overhead of Multiprocessor Prefetchers. In *Proceedings of the 18th International Parallel and Distributed Processing Symposium (IPDPS 2004)* (Santa Fe, New Mexico, USA, Apr. 2004).

[47] Wallin, D., Johansson, H., and Holmgren, S. Cache Memory Behavior of Advanced PDE Solvers. Tech. Rep. 2003-044, Department of Information Technology, Uppsala University, Aug. 2003.

[48] Wallin, D., Johansson, H., and Holmgren, S. Cache Memory Behavior of Advanced PDE Solvers. In *Processing of Parallel Computing 2003 (ParCo2003)* (Dresden, Germany, Sept. 2003).

[49] Wallin, D., Zeffer, H., Karlsson, M., and Hagersten, E. Vasa: A Simulator Infrastructure with Adjustable Fidelity. In *Proceedings of the 17th IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS 2005)* (Phoenix, Arizona, USA, Nov. 2005).

[50] Zeffer, H. *Hardware-Software Tradeoffs in Shared-Memory Implementations.* Licentiate thesis, Department of Information Technology, Uppsala University, May 2005.

[51] Zeffer, H., and Hagersten, E. Adaptive Coherence Batching for Trap-Based Memory Architectures. Tech. Rep. 2005-016, Department of Information Technology, Uppsala University, May 2005.

[52] Zeffer, H., and Hagersten, E. A Case For Low-Complexity Multi-CMP Architectures. Tech. Rep. 2006-031, Department of Information Technology, Uppsala University, June 2006.

[53] Zeffer, H., Radović, Z., Grenholm, O., and Hagersten, E. Evaluation, Implementation and Performance of Write Permission Caching in the DSZOOM System. Tech. Rep. 2004-005, Department of Information Technology, Uppsala University, Feb. 2004.

[54] Zeffer, H., Radović, Z., Grenholm, O., and Hagersten, E. Exploiting Spatial Store Locality through Permission Caching in Software DSMs. In *Proceedings of the 10th International Euro-Par Conference (Euro-Par 2004)* (Pisa, Italy, Aug. 2004).

[55] Zeffer, H., Radović, Z., and Hagersten, E. Flexibility Implies Performance. Tech. Rep. 2005-013, Department of Information Technology, Uppsala University, Apr. 2005.

[56] Zeffer, H., Radović, Z., and Hagersten, E. Exploiting Locality: A Flexible DSM Approach. In *Proceedings of the 20th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2006)* (Apr. 2006).

[57] Zeffer, H., Radović, Z., Karlsson, M., and Hagersten, E. TMA: A Trap-Based Memory Architecture. Tech. Rep. 2005-015, Department of Information Technology, Uppsala University, May 2005.

[58] Zeffer, H., Radović, Z., Karlsson, M., and Hagersten, E. TMA: A Trap-Based Memory Architecture. In *Proceedings of the 20th International Conference on Supercomputing* (June 2006).